Experiment-4

Multi-Stage Amplifiers

Introduction

The objectives of this experiment are to examine the characteristics of several multi-stage amplifier configurations. Several of these will be breadboarded and measured for voltage gain, frequency response and signal swing.

In addition to the performance measurements, you should also pay attention to how the biasing of each amplifier stage is achieved, how the signal is coupled from stage to stage, and what design strategy has been adopted to desensitize the amplifier performance to variations in the transistor parameters. For each amplifier in this experiment, try to answer the question: "What has been achieved by connecting the transistors in this configuration?" To begin to answer this question, first identify whether a particular transistor is providing bias stabilization for other transistors, or is a gain stage in the signal path. Some transistors may simultaneously function in both roles. Then try to determine what components set the voltage gain of the amplifier. Track the path of the signal through the different stages of the amplifier and try to understand how much voltage gain is produced across each stage, how big the signal is at each node along the path, and what limits the signal swing at each node. Draw a schematic of the amplifier in your lab notebook and mark it up extensively to show the DC bias voltage at each node, the path that the signal takes from input to output, and any thing else that is of interest to you.

The amplifier circuits described in this experiment are not as simple as those previously used in this lab. While all of the component values are fairly close to the values needed to make the circuits work, normal variations in transistor parameters will require that each amplifier circuit be "tuned-up" slightly to center the signal swings or trim out the gain. This is left for you to do without any explicit instructions and is intended to force you to understand how the circuits work and to gain skill in electronic troubleshooting. Similarly, the procedures will only ask you to measure certain performance parameters without giving explicit instructions. At this point, you should be comfortable making all of these measurements. Refer back to experiments 2 and 3 if you need to refresh your memory on making gain and frequency response measurements.

Procedure 1 Wideband CE-EF amplifier

Comment

A common-emitter (CE) stage is one of the most widely used BJT configurations for obtaining both voltage and current gain. However, its gain is proportional to the resistance on its collector. Attaching a heavy load (low resistance) will thus reduce the gain. One simple means for improving on this is to buffer the output voltage with an emitter-follower (EF) stage, also known as a common-collector stage.

Set-Up

Using the solderless breadboard, construct the circuit shown in Fig. E5.1 using the following components:

R1 = 1.0 kΩ 5% 1/4 W
R2 = 6.8 kΩ 5% 1/4 W
R3, R5 = 3.3 kΩ 5% 1/4 W
R4 = 100 Ω 5% 1/4 W
C1, C2 = 10 µF electrolytic
Q1, Q2, Q3 = CA3046 npn BJT array

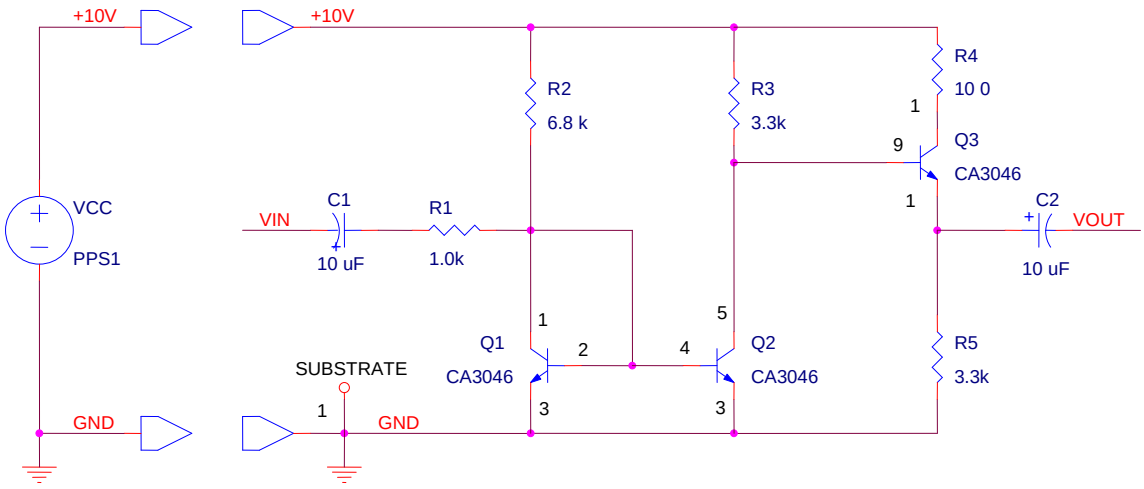

Figure E4.1

Configure the PPS1 DC power supply to implement the VCC = +10.0 V DC power supply rail, as shown in Fig. E4.1. Turn the PPS1 DC power supply on.

Configure the signal generator to output a 1.0 kHz sinewave with a peak-to-peak amplitude of 1.0 Vpp. Input the signal to the free end of C1, with the signal generator ground being connected to the ground rail of the amplifier.

Configure an oscilloscope to measure voltage versus time on both Ch-1 and Ch-2. Start off with 5 V/div and DC coupling for both channels to probe the signal swings and biasing. Increase the sensitivity and use AC coupling to probe the signal amplitude. Attach both probe grounds to the ground rail of the amplifier.

Measurement-1 Adjust the circuit and signal generator to produce clean 1.0 kHz sinewaves on the input and output. Measure and record the amplitude of both input and output, and then take the ratio to determine the voltage gain.

Increase the frequency of the signal generator until the voltage gain falls to 70 percent of its value at 1.0 kHz. Measure and record this -3 dB bandwidth of the amplifier.

Restore the frequency to 1.0 kHz, and increase the amplitude of the signal generator until the output signal is clipped at both the positive and negative peaks. Measure and record the output voltage levels at which clipping occurs (two voltages – one for negative clipping and one for positive clipping).

Question-1 (a) Explain how the Q1-Q2 pair sets the bias level for Q3.
(b) Explain why the voltage gain of this amplifier is approximately given by R3/R1.
(c) Explain what sets the clipping levels for this amplifier.

Procedure 2 Active loads---a simple opamp

Comment

An active load usually refers to the use of a transistor's output characteristics (I_C versus V_{CE}) to provide a high output resistance but at a much larger level of DC current than what a passive resistor alone could provide. Using an active load for a common-emitter stage greatly increases the voltage gain since the collector resistance for the CE amplifier stage is now the output resistance of the active load transistor. In the circuit of Fig. E4.2, an active load is used on both collector legs of an npn differential pair. When connected like a current mirror as shown, the pair of active loads also has the benefit of routing both sides of the differential signal into the next stage, the base of Q6. The active loads in this case form a differential to single-ended converter.

Transistor Q3 provides an improved current source for the differential pair which greatly increases the common-mode rejection ratio.

Transistor Q6 implements a simple common-emitter stage with a load resistor of R8. This adds some final gain and current drive to the output pin. Resistors R5-R6-R7 provide bias stabilization for this output stage.

R4 is an optional trimpot between the emitters of Q1 and Q2. This will lower the voltage gain of this stage slightly, but it will allow the input differential amplifier to be balanced to help bias the circuit so that the output voltage will be about zero when the differential input voltage is also zero. This may or may not be necessary. If R4 is used, its value should not be more than 1.0 kΩ, or the gain of the differential amplifier will be lowered too much.

Set-Up

Construct the circuit shown in Fig. E4.2 on your solderless breadboard using the following components:

R1 = 10 kΩ 5% 1/4 W
R2 = 100 kΩ 5% 1/4 W
R3 = 1.0 kΩ 5% 1/4 W
R4 = 1.0 kΩ trimpot (if needed to balance the amplifier)
R5 = 15 kΩ 5% 1/4 W
R6 = 43 kΩ 5% 1/4 W
R7 = 620 Ω 5% 1/4 W
R8 = 3.3 kΩ 5% 1/4 W
Q1, Q2, Q3 = 2N3904 npn BJT
Q4, Q5, Q6 = 2N3906 pnp BJT

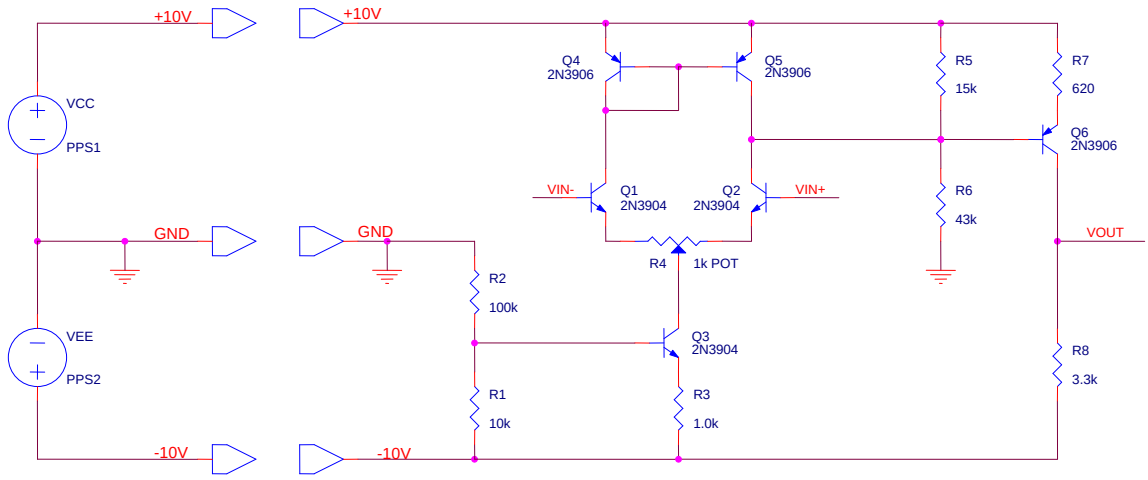

Figure E4.2

Configure the PPS1 DC power supply to +10.0 V DC and the PPS2 DC power supply to -10.0 V DC. Connect the PPS1 and PPS2 outputs to the breadboard. The GND terminals on PPS1/PPS2 are the system ground.

Because of the high gain of this circuit, you may need to adjust the DC balance of the input differential amplifier. First check the balance by grounding both inputs to the bases of Q1 and Q2. Make certain that these grounds go to the system ground labeled GND in Fig. E4.2. With both inputs grounded, measure the voltage on the output pin, connected to the collector of Q6. This should be within a volt or so of ground, also. If it is not, then you may need to add in the optional trimpot R4 between the emitters of Q1 and Q2. Power down the circuit, install R4, and then fire it back up to re-measure the DC output voltage. If the output voltage is still not sufficiently close to zero, adjust the trimpot to center the output voltage to zero. You may need to readjust this balance as you go through the rest of this procedure.

Measurement-2 Ground the (–) input of the amplifier and apply a sinewave to the (+) input, relative to the system ground. Adjust the amplitude of the input to produce a non-distorted sinewave at the output. Adjust the frequency so that the maximum voltage gain is obtained. You will have to use a very small amplitude sinewave on the input, since the voltage gain of this circuit is rather high, and the frequency that you use may need to be fairly low to obtain the maximum voltage gain. Measure and record the amplitude of the input and output

sinewaves, and take their ratio to determine the differential-mode voltage gain.

Increase the amplitude of the signal generator to where the output waveform is clipped at both the positive and negative peaks. Measure and record the output voltage levels at which the clipping occurs.

Decrease the amplitude of the signal generator to again produce an undistorted sinewave at the output and then increase the frequency to where the voltage gain drops to 70 percent of its maximum value. Measure and record this frequency as the -3 dB differential-mode bandwidth.

Release the (–) input from ground and apply the signal generator output to both the (+) and (–) inputs simultaneously, adjusting the amplitude to produce an undistorted sinewave at the output. Measure and record the amplitude of the input and output sinewaves and take their ratio to determine the common-mode voltage gain.

Question-2

(a) From your measured data, calculate the differential-mode voltage gain of the amplifier in decibells (dB).
(b) From your measured data, calculate the common-mode voltage gain of the amplifier in decibells (dB).
(c) Calculate the common-mode rejection ratio (CMRR) for this amplifier, expressing the result in decibells (dB).
(d) Explain what determines the clipping voltage levels.

Procedure 3 Complementary class-AB output stage

Comment

Emitter followers (or common-collector) stages were shown to be a nice means for increasing the output current level of an amplifier and buffering voltage gain stages. However, when a large bias current runs continuously through such a stage, it dissipates far more power than it delivers to the load, resulting in poor power efficiency. One way to correct this is to only operate the transistor when it is delivering current to the load, termed class-AB operation. Using two transistors of opposite sex but driven by the same input signal is termed a complementary output stage and provides a power efficient configuration for output buffering or current boosting. This circuit can be used to boost the output current of an opamp. Putting the output stage inside the feedback loop causes the gain of the opamp to linearize the characteristics of the output stage.

Set-Up

Construct the circuit shown in Fig. E4.3a on a solderless breadboard using the following components:

R1, R2 = 4.7 kΩ 5% 1/4 W
R3, R4 = 5.0 Ω 5% 1/4 W
R5 = 100 kΩ 5% 1/4 W
RL = 100 Ω 5% 1/4 W
C1, C2 = 10 µF electrolytic
D1, D2 = 1N914 or 1N4148
Q1 = TIP-29 npn power BJT
Q2 = TIP-30 pnp power BJT
Q3 = 2N3904 npn BJT
Q4 = 2N3906 pnp BJT

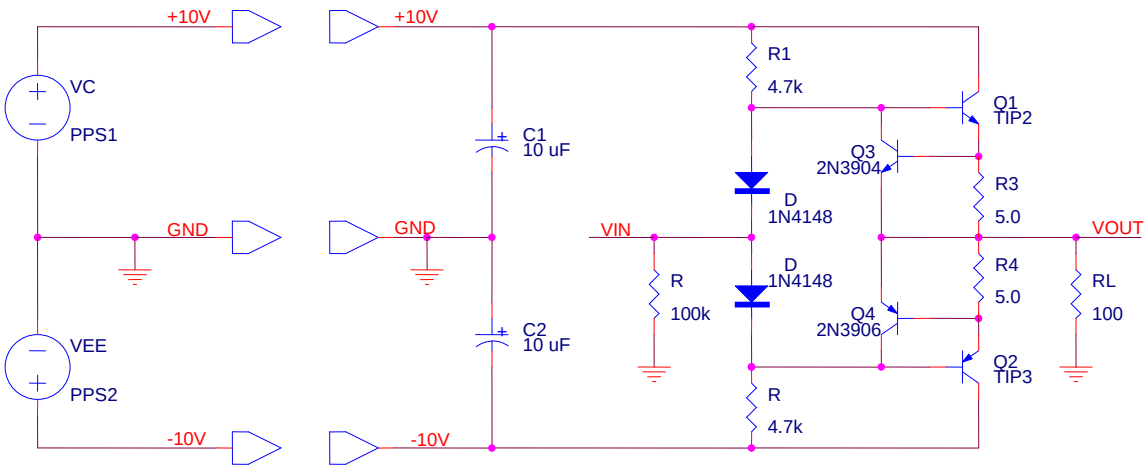

Figure E4.3a

Configure PPS1 and PPS2 to implement the VCC = +10.0 V and VEE = −10.0 V DC power supply rails, as shown in Fig. E4.3a. Turn the PPS power supplies ON. The center ground terminal is the system ground.

Configure the signal generator to produce a 1.0 kHz 5.0 Vpp amplitude sinewave and apply this sinewave across the input resistor R5.

Measurement-3a Use an oscilloscope to monitor the input and output voltage waveforms. Record sketches of the input and output waveforms in your lab notebook.

Increase the amplitude of the input signal until the output voltage waveform is clipped on both the positive and negative peaks. Measure and record the output voltage clipping levels.

Restore the input signal to a 1.0 kHz 5.0 Vpp amplitude sinewave and increase the frequency until the output voltage waveform falls to 70 percent of its previous amplitude. This is the -3 dB bandwidth of the output stage.

Question-3a (a) Calculate the voltage gain for this output stage.
(b) Comment on any distortion that is seen in the output voltage waveform.
(c) Calculate the limited value of output current when the short-circuit protection becomes active.

More Set-Up Modify the circuit of Fig. E4.3a to that of Fig. E4.3b by adding an opamp and a feedback loop.

R1, R2 = 4.7 kΩ 5% 1/4 W
R3, R4 = 5.0 Ω 5% 1/4 W
R5 = 100 kΩ 5% 1/4 W
RL = 100 Ω 5% 1/4 W
C1, C2 = 10 μF electrolytic
D1, D2 = 1N914 or 1N4148
Q1 = TIP-29 npn power BJT
Q2 = TIP-30 pnp power BJT
Q3 = 2N3904 npn BJT
Q4 = 2N3906 pnp BJT
U1 = UA741C opamp

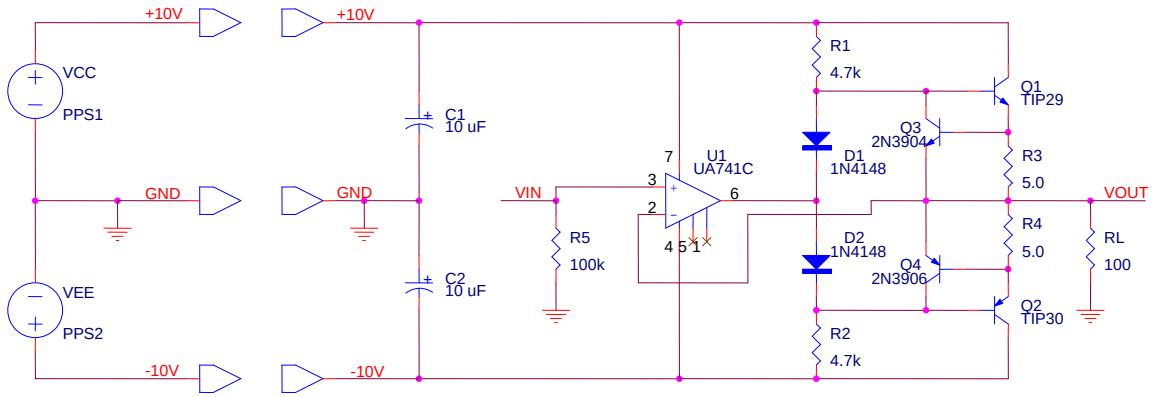

Figure E4.3b

Measurement-3b Apply a 1.0 kHz 5.0 Vpp sinewave to the input and use an oscilloscope to monitor the input and output voltage waveforms. Record sketches of the input and output waveforms in your lab notebook.

Increase the amplitude of the input signal until the output voltage waveform is clipped on both the positive and negative peaks. Measure and record the output voltage clipping levels.

Restore the input signal to a 1.0 kHz 5.0 Vpp amplitude sinewave and increase the frequency until the output voltage waveform falls to 70 percent of its previous amplitude. This is the -3 dB bandwidth of the overall circuit.

Question-3b (a) Calculate the voltage gain of the overall circuit.
(b) Compare the clipping levels and bandwidth of the circuit to that of the output stage without the opamp.
(c) Compare the distortion of the opamp circuit to that of the output stage without the opamp. What are the tradeoffs?