**Laboratory-3**

**JFET and MOSFET Characterization**

**Introduction**

The objectives of this experiment are to observe the operating characteristics of junction field-effect transistors (JFET's) and metal-oxide-semiconductor field-effect transistors (MOSFET's). Some basic methods for extracting device parameters for circuit design and simulation purposes are also examined.

**Precautions**

Junction field-effect transistors (JFET's) involve only an internal pn-junction and are thus relatively static insensitive and may be handled freely. However, MOSFET's involve a very thin gate oxide layer which may not have any static protection diodes included as part of the device. As a result, MOSFET's can be very static sensitive and must be treated properly to avoid having to buy replacements.

To avoid static discharge damage to MOSFET's, keep their leads inserted into black conductive foam whenever possible. Always touch a grounded object, such as the frame of the lab bench, to discharge any built-up static charges from your body before handling the MOSFET. After this, carefully remove the MOSFET from the black foam and insert it into either the curve tracer or the solderless breadboard. Pay particular attention to correctly identifying the leads on the devices. Improper connection of the device is another means in which they can be destroyed. Once the MOSFET is correctly connected into its test circuit, it is reasonably well protected from static, since there now exist resistors or power supply terminals which allow current to flow from lead to lead. As a basic rule, remember that static electricity affects only floating terminals on a device or circuit. Simply connecting these floating terminals to ground with a large value resistor, say 1 MΩ or so, is often sufficient to provide a discharge path for any built-up charges.

If you are still having difficulty in keeping the MOSFET's from being destroyed by static, you may wish to try another trick which works well for very sensitive parts. While the MOSFET is still plugged into the conductive black foam, take a 1-2 inch long piece of very fine bare copper wire and wrap it around all of the leads, just below the lip of the case, so that it shorts all of the leads together. (Some discrete MOSFET's even come with a piece of wire around the leads for this purpose.) Twist the free ends of the wire together so that it will not fall off. After the leads have all been shorted together by the wire, remove the MOSFET from the black foam and re-insert it into either the curve tracer or the solderless breadboard. Finish all of the rest of the circuit connections and instrument set-ups, and then only before you test the circuit, remove the bare copper shorting wire. Re-wrap the MOSFET leads...
with the bare copper shorting wire before removing it from the breadboard or test fixture.

Electrostatic discharge (ESD) can very frequently arise from a human body transferring a static electric charge to the circuit or device. It has been found that the human body acts like a small capacitance relative to the Earth ground, and when discharged into a circuit, the current is limited by the tissue and skin impedance. The standardized human body model (HBM) for electrostatic discharge simulation consists of a 100 pF capacitor in series with a 1.5 kΩ resistor. The 100 pF capacitor can become charged to fairly high voltages by comparatively simple actions, as shown in the following table, taken from the Motorola Power MOSFET Data Book:

<table>
<thead>
<tr>
<th>Action</th>
<th>Electrostatic Voltage: 10-20 % rel. humid. (V)</th>
<th>Electrostatic Voltage: 65-90 % rel. humid. (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>walk on carpet</td>
<td>35,000</td>
<td>1,500</td>
</tr>
<tr>
<td>walk on vinyl floor</td>
<td>12,000</td>
<td>250</td>
</tr>
<tr>
<td>work at bench</td>
<td>6,000</td>
<td>100</td>
</tr>
<tr>
<td>handle vinyl envelope</td>
<td>7,000</td>
<td>600</td>
</tr>
<tr>
<td>pick up poly bag</td>
<td>20,000</td>
<td>1,200</td>
</tr>
<tr>
<td>shift position in foam chair</td>
<td>18,000</td>
<td>1,500</td>
</tr>
</tbody>
</table>

A relative humidity of 10-20 % is extremely dry (and almost never occurs in Seattle), while relative humidity in the range of 65-90 % is more typical for the Pacific Northwest. Thus, our ESD problems are quite tame compared to the situation in the dry Southwest of the United States.

MOSFET arrays are integrated circuits which contain several MOSFETs fabricated into a common silicon substrate. Most of the time, the gates of these MOSFETs are internally protected from ESD by clamping diodes to both the upper and lower power supply rails. If the voltage on the gate pin exceeds the upper power supply rail by $V_{on}$, then the upper clamp diode will turn on and keep the voltage from rising further. If the voltage on the gate pin falls below the lower power supply rail by $V_{on}$, then the lower clamp diode will turn on and keep the voltage from falling further. In this manner the input gate voltages are clamped within the range of $V_{SS} - V_{on}$ to $V_{DD} + V_{on}$. MOSFET arrays with internal clamping diodes are fairly safe to handle and are much more robust than individual discrete MOSFETs which have no gate protection. The CD4000 family CMOS logic integrated circuits used in this and the other experiments have these ESD input protection diodes.
Procedure 1  Discrete MOSFET gate lead, sex, and mode identification

Comment  
The objective of this procedure is to learn how to identify the leads, the sex, and the mode of a MOSFET using only a digital multimeter (DMM). The method for achieving this is based upon looking for pn-junctions and insulating oxide layers between the different pairs of terminal leads. Thus, one should first become familiar with using a DMM to find these junctions.

Practice  
Turn on a bench DMM and configure it to measure (two wire) resistance. Plug a black squeeze-hook test lead into the negative banana jack of the meter and a red squeeze-hook test lead into the positive banana jack of the meter. Locate a 1N4148 diode from the parts kit and measure its resistance with the DMM in both the forward and reverse bias directions. Note that the red lead from the positive input of the DMM is the one which will have the more positive voltage for this test. Record these readings in your lab notebook, and note these readings as being typical for a forward and reverse biased pn-junction. You can then refer to these readings to determine the polarity of pn-junctions that exist between pairs of leads of a MOSFET.

Comment  
Most modern DMM’s perform resistance measurements with a very small test voltage, in order to minimize battery drain. As a result, this test voltage may be insufficient to turn on a pn-junction, rendering the meter useless for this application. Many modern DMM’s offer a special range position as part of the resistance mode which uses a larger test voltage of 1.5 to 2.5 V to turn on a given pn-junction diode. More advanced DMM’s have a diode test position which displays the diode’s forward turn-on voltage when a current of a few mA is passed through it. This range is usually indicated by a small diode symbol on the selector switch. When the pn-junction is forward biased, the meter will read the diode’s turn-on voltage, while when reverse biased, the meter will read the open-circuit test voltage across the diode, which is usually 2.0 V or greater. Hence, in a diode test mode, the larger voltage reading indicates the reverse-bias polarity of the diode, while a forward-bias polarity of the diode would be indicated by a typical turn-on voltage of about 0.6 Volts or so.

Practice  
Next, if your DMM has this feature, select the diode test function on the DMM, as identified by the small diode symbol next to it. Measure the voltage across the 1N4148 diode when forward and reverse biased, and record these in your laboratory notebook as typical values. These readings will help you to identify pn-junctions in other devices.

Comment  
Very old volt-ohm-ammeters (VOM’s), such as the classic model 206 Simpson and other D’Arsonval movement meters (those with a mechanical needle and
scale), usually implemented the ohms function with an internal 1.5 V battery which made the red lead more negative than the black lead. As a result, when using one of these meters to determine diode polarities, one must mentally reverse the lead polarities in order to obtain the correct deductions from the readings. On most modern DMM's, including handhelds, the red and black leads do have the correct voltage polarity in the ohms mode, i.e. red being more positive than black.

**Set-Up**

Locate a type 2N7000 MOSFET from the parts kit. This should be a three lead device in a small plastic TO-92 package. Insert the device into a solderless breadboard; this will help keep the part positioned while the various lead combinations are probed with the DMM test leads. You might find that a few short jumper wires are also useful for quickly connecting the device to the DMM test leads. The objective of this procedure will be to determine as much information as possible about an “unknown” MOSFET, using only simple DMM measurements.

**Measurement-1**

The gate lead of a MOSFET is separated from the other leads by the gate oxide layer which forms the gate of a MOS capacitor. For DC, this capacitor should not pass any current. Thus, use the DMM in the resistance mode to find the lead on the 2N7000 MOSFET which does not conduct to any of the other leads, in either polarity.

With the gate lead identified, it stands to reason that the remaining leads must be the drain and the source. The 2N7000 MOSFET happens to have a special internal diode which guards against the drain being taken more negative than the source, as shown in Fig. E3.1. (This situation can occur during transient switching of an inductive load, and the internal diode is present to protect against this.) The body of the MOSFET is also internally connected to the source lead, effectively making the four terminal MOSFET a three terminal part.

![Figure E3.1](image)

Switch the DMM to the diode test function and determine the source and drain leads from the direction that the transient protection diode allows...
current to pass (from source to drain). For the 2N7000 MOSFET, this also verifies that it is an n-channel device.

More conventional MOSFETs which do not have either the transient protection diode or their body and source tied together (a true four-terminal MOSFET) would show the source and drain as symmetrical in so far as any DMM measurements are concerned. For such devices, the polarity of the body diode would be used to identify the body terminal and also whether the MOSFET was n-channel or p-channel.

With all three leads of the 2N7000 MOSFET now identified, short the gate and source leads together with a small jumper wire on the solderless breadboard. This is to guarantee that $V_{GS} = 0$. Use the DMM to measure the conduction from drain to source. If this is significant, then the device channel is turned on without any gate bias, and the MOSFET is a depletion mode (D-mode) or “normally-ON.” If the conduction from drain to source with $V_{GS} = 0$ is negligible, then the MOSFET is an enhancement mode (E-mode) or “normally-OFF.” Make this determination for the 2N7000 MOSFET and record the results in your laboratory notebook.

Question-1
(a) From your measurements above, summarize your findings about the given 2N7000 MOSFET in your notebook.
(b) Draw a picture of the device package and label the leads. (It is conventional to do this with a view of the device looking down on it with the leads pointing away from you, as if it were soldered into a printed circuit board. This is usually termed a component-side view, in reference to the component side of the circuit board.)
(c) Look up the data sheet for the the 2N7000 and compare your deductions with the manufacturer's specifications. (Data sheets can be most easily obtained online from the EE Stores web pages.) Comment on any discrepancies.
(d) Draw up a flow chart for testing any four-terminal MOSFET with an ohmmeter which can be used to conclusively determine which lead is the gate, which lead is the body, whether the device is an n-channel or p-channel, and whether the device is a D-mode or an E-mode.
(e) If the gate oxide were destroyed by a static electricity discharge, speculate on how the DMM readings might be different from those that were observed.
**Procedure 2  Integrated MOSFET lead, sex, and mode identification**

**Comment**

This procedure will use the CD4007 CMOS integrated circuit. This is a very general purpose CMOS IC which includes an array of 3 n-channel and 3 p-channel MOSFET’s connected as shown in Fig. E3.2a. The digits by each terminal indicate the pin numbers on the 14-pin DIP package, shown in Fig. E3.2b. Note that pin 14 (VDD) must *always* be connected to the most positive power supply voltage, and pin 7 (VSS) must *always* be connected to the most negative (or ground) power supply voltage in order to keep the body-source and body-drain pn-junctions from becoming forward biased. This is what provides electrical isolation between the different MOSFETs in the integrated circuit, and if this isolation fails, all of the MOSFETs end up being shorted together with completely unpredictable results. Although it is not shown in the schematic, each of the three inputs to the MOSFET gates (pins 3, 6, & 10) have two ESD protection diodes that connect them to the VDD and VSS power rails.

![Figure E3.2a](image_url)

**Set-Up**

Locate the CD4007 CMOS array integrated circuit. Plug the CD4007 into the solderless breadboard so that it straddles the center groove. This procedure will perform tests only on MOSFET M2 in Figure E3.2a. You may find it helpful to plug short jumper wires into the solderless breadboard to contact pins {3,4,5,7, & 14} of the integrated circuit. All of the next measurements will involve only these leads.
Turn on a bench DMM and configure it to measure resistance in a two wire mode. Plug a black squeeze-hook test lead into the negative banana jack of the meter and a red squeeze-hook test lead into the positive banana jack of the meter. The objective of this procedure will be to verify the leads, sex, and mode of the MOSFET using only the ohmmeter function of the DMM.

Consider only pins \{3,4,5, & 7\} of the IC which connect to the \{G,S,D & B\} of MOSFET M2. First, the identification of these leads will be verified. A MOSFET gate is normally completely isolated from the other electrodes by a thin insulating layer of silicon dioxide. On a discrete MOSFET that has no internal gate protection diodes, a DMM in its ohmmeter setting can be used to first find the gate lead as the one which does not have conduction to any other lead in either polarity. For the CD4007 CMOS array, the presence of the internal gate protection diodes complicates the problem of identifying the gate lead. For this situation, it is usually easier to identify the body lead first. Because of the presence of the ESD protection diodes on the gate, the body at VSS will conduct to the gate through one diode, and the gate will conduct to the upper VDD rail through the other diode. However, the body terminal is unique, because it will exhibit conduction from the body to each of the other three terminals when the body is the more positive terminal.Probe different pairs of leads (pins 3,4,5, & 7) with the DMM to find the one pin which conducts (like a forward biased pn-junction) to each of the other three. Since this corresponds to current going into the body terminal, this also verifies that the MOSFET is an n-channel, since its body must be p-type for this to occur.

With the body lead identified, the gate lead can then be identified next, because of the electrical symmetry between the drain and source. Because the voltage used by the DMM in the diode test function can easily turn on the MOSFET channel, the best method to identify the gate is to find the terminal which, when shorted to the body with a jumper, causes the other two terminals to show symmetric electrical behavior. That means that when the gate is shorted to the body, the channel of the MOSFET should be non-conducting, and the only conduction involving the source and drain should be through the source-body and drain-body pn-junctions. Test the MOSFET M2 with the DMM and a short jumper wire to identify the gate in this manner.

With the gate and body leads identified, the remaining two leads must therefore be the drain and source. Now use the DMM, again in its ohmmeter setting, to determine whether the device is a depletion-mode (D-mode, or normally-ON) or an enhancement-mode (E-mode, or normally-OFF) device. Because the gate could have picked up a stray charge that has not fully
dissipated, one must insure that the gate bias is at zero. This is done by using a small jumper wire to short the gate to the body, giving $V_{GB} = 0$, similar to the connection used previously to identify the gate lead.

As mentioned, the gate of MOSFET M2 has two ESD protection diodes, one to VDD and the other to VSS. If the gate (pin 3) is taken to a voltage higher than VDD (pin 14), then the ESD protection diode between the two will turn on, clamping the voltage difference to the diode turn-on voltage. Use the DMM in the diode test function to verify the presence of the ESD protection diode between the gate and VDD.

**Question-2**
(a) From your measurements above, summarize your findings about MOSFET M2 in your notebook.
(b) Draw a schematic of MOSFET M2 and its two gate protection diodes and label the MOSFET leads.
(c) Is it possible to distinguish the drain lead from the source lead using only an ohmmeter? Explain why or why not.
(d) If the power leads to the CD4007 IC are reversed, with VSS at a higher potential than VDD, then other pn-junction diodes can be turned on, clamping this voltage to the diode turn-on voltage. Using the schematic of Fig. E3.2a, show how current can flow from VSS to VDD and create a voltage drop of two diode turn-on voltages (about 1.2 V).
**Procedure 3 Measurement of I-V Characteristics of a MOSFET**

**Comment**
To characterize a multi-lead semiconductor device such as a MOSFET, we would like to be able to know and predict the currents through each lead as a function of the voltages between each of the leads. Since the gate lead does not allow any DC current to pass, and the body will be non-conducting when the body diodes are reverse-biased, the only current to consider in a normally functioning MOSFET is the channel current flowing from drain to source, $I_D$. But this is still a function of the three terminal voltages, $V_{GS}$, $V_{DS}$, and $V_{BS}$. The $V_{BS}$ dependence is the weakest, and we shall suppress it for the time being by keeping $V_{BS} = 0$. The normal manner for displaying the characteristics of the MOSFET involving $I_D$ as a function of $V_{GS}$ and $V_{DS}$ is to plot several curves of $I_D$ versus $V_{DS}$ on these axes for selected values of $V_{GS}$. These are termed the output characteristics. The other way is to plot $I_D$ versus $V_{GS}$ on these axes for selected values of $V_{DS}$. These are termed the transfer characteristics. The objective of this procedure will be to measure and record the output characteristics of a MOSFET.

**Set-Up**
The first part of setting up the hardware is to build the MOSFET circuit as shown below in the schematic of Fig. E3.3a.

![Schematic of Fig. E3.3a](image)

The excitation voltage $V_{DD}$ is from DC power supply. This voltage is applied across the series connection of a current limiting resistor $R_C = 100 \, \Omega$, the drain-source leads of the device under test (DUT), and the drain current sensing resistor $R = 100 \, \Omega$. Thus, $V_{DD} = V_{DS} + V_{RC}$.

The voltage of DMM1 is equivalent to the voltage $V_{RC}$, while the voltage from DMM2 is the voltage $V_{DS}$. 

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Measurement-3
This experiment requires two variable DC power supplies. The Eleco power supply has only one variable DC output whose value ranges from 0-20v. However, there are three other fixed output DC sources (5v, 12v and -12v). We are going to use the 5v DC source and a 10K potentiometer to construct a voltage divider whose output ranges from 0-5v. Set up the voltage divider circuit and use it as DC power supply 2 in the procedure below.

Adjust the DC power supply 2 VGG to produce voltages +1.0 Volts. Then adjust DC power supply 1 from 0.0 V to 10.0 V with increment 1.0 V. Verify both voltage remain at the adjusted value, if not readjust. Measure the VRC and VDS with DMMs. If two DMMs are not available at your lab bench, you may have to switch back and forth between the two terminals at DMM1 and DMM2. Record the drain current and VDS in a table in your notebook. The drain current is equal to VRC/100.0. Increase the DC power supply 2 in steps of 0.5 V and repeat till measuring four different (ID,VDS) pairs.

Tabulate your result in your report and using some graph paper, plot the I-V characteristics (ID vs VDS) of MOSFET.

Question-3
(a) Scan through the measurement results and find the value of VGS which just starts to produce a non-zero drain current. This is a first approximation to the threshold voltage VT of the MOSFET under test.
(b) Pick a few values of VGS for which the drain current ID shows a clearly defined saturation. Find the value of VDS at which the drain current ID reaches its saturation value and then compare this actual value of VDS,sat to a computed value of VGS – VT. Comment on how close these values agree.
(c) Using an electron mobility value of \( \mu_n = 800 \text{ cm}^2/\text{V-s} \) and a gate oxide thickness of \( x_{ox} = 80 \text{ nm} \), compute the value of \( k = \mu_n C_{ox} \) and from this value and a few of the measured data points (where the drain current is saturated) make a rough estimate of the W/L ratio for the 2N7000 MOSFET. Does this W/L ratio seem reasonable?
Procedure 4  Output conductance effects

Measurement-4 Locate a 10 kΩ 5% 1/4 W resistor, and connect this resistor in parallel with the drain and source terminals of the MOSFET on the solderless breadboard (pins 7 & 8). This resistor simulates the effect of increasing the output conductance of the MOSFET. Repeat previous procedure to produce (ID, VDS) plots.

Question-4 (a) First discuss qualitatively what effect the addition of the 10 kΩ resistor has on the MOSFET output characteristics. (b) From the first measurement of MOSFET M1 without the resistor being present, and select a value of V_{GS} which shows a clean saturation of the drain current. Select a few points within the saturated region of the curve and calculate the slope of the output characteristics in units of Ω^{-1}. Then take the reciprocal of this value to obtain the inverse slope in units of Ω. These values are the output conductance and resistance, respectively. (c) Next from the second measurement of MOSFET M1 with the resistor added, and perform the same analysis on the same V_{GS} curve to find the output conductance and resistance for this case. (d) Discuss how closely these measured values match to the empirical device equation

\[ I_{\text{Dsat}} = 0.5 \, k(V_{\text{GS}} - V_{\text{T}})^2 \, (1 + \lambda V_{\text{DS}}) \]

where \( \lambda \) is the output conductance parameter in units of V^{-1}. 
Procedure 5  
**JFET gate lead, sex, and mode identification**

**Set-Up**  
Locate a type MPF102 JFET from the parts kit. This should be a three lead device in a small plastic TO-92 package. Turn on a bench DMM and configure it to measure (two wire) resistance. Plug a black squeeze-hook test lead into the negative banana jack of the meter and a red squeeze-hook test lead into the positive banana jack of the meter. The objective of this procedure will be to determine which lead of the JFET is the gate, whether the JFET is an n-channel or p-channel, and whether the JFET is an E-mode or D-mode device using only the ohmmeter function of the DMM.

**Measurement**  
A JFET uses a single pn-junction between the gate and the drain/source terminals to modulate the channel conductance. Use the DMM in its ohmmeter setting to test pairs of leads on the JFET and therefore identify the gate lead on the device. From the polarity which causes the gate terminal to conduct, deduce whether the JFET is an n-channel or p-channel device.

With the gate lead identified, it stands to reason that the remaining leads must be the drain and the source. Use the DMM, again in its ohmmeter setting, to determine whether the device is a depletion-mode (D-mode, or normally-ON) or an enhancement-mode (E-mode, or normally-OFF) device.

**Question**  
(a) From your measurements above, summarize your findings about the given MPF102 JFET in your notebook.
(b) Draw a picture of the device package and label the leads.
(c) Is it possible to distinguish the drain lead from the source lead using only an ohmmeter? Explain why or why not.
(d) Look up the data sheet for the the MPF102 and compare your deductions with the manufacturer’s specifications. (MPF102 is a Motorola part number, but it is also second sourced by Fairchild.) Comment on any discrepancies.
(e) Draw up a flow chart for testing any JFET with an ohmmeter which can be used to conclusively determine which lead is the gate, whether the device is an n-channel or p-channel, and whether the device is a D-mode or an E-mode.