

NSF Center for High-Performance Reconfigurable Computing (CHREC)

University of Florida, Alan George, 352.392.5225, george@hcs.ufl.edu

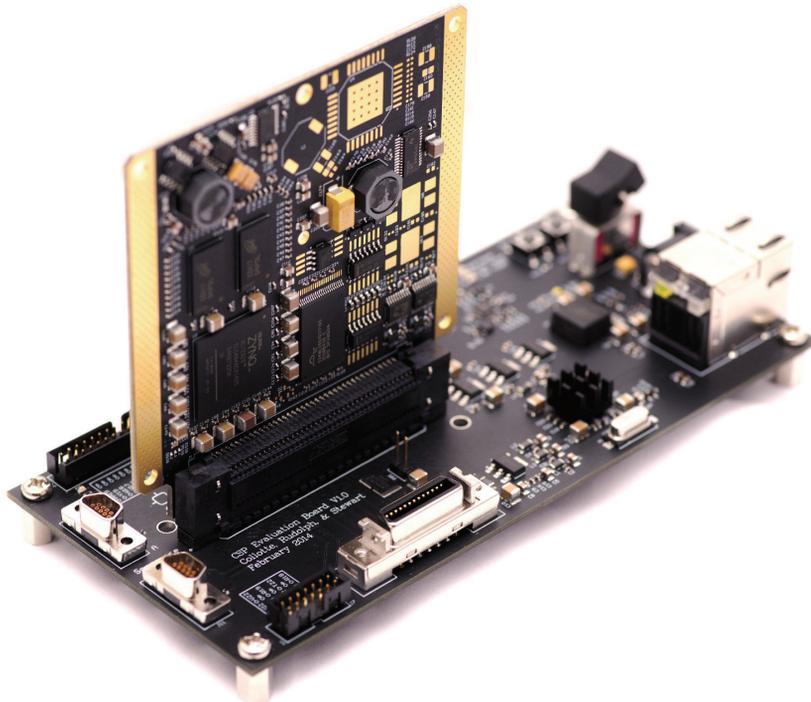
University of Florida, Herman Lam, 352.392.2689, hlam@ufl.edu

Brigham Young University, Mike Wirthlin, 801.422.7601, wirthlin@ee.byu.edu

Virginia Tech, Peter Athanas, 540.392.7250, athanas@vt.edu

CHREC Space Processor (CSP)

For over a half century the U.S. space program has been a leading contributor to the health and growth of our nation from the perspectives of science, technology, economy, and defense. Given the nature and purpose of present and future spacecraft, be they for earth science, space science and exploration, or defense surveillance, one of their most daunting challenges is on-board computing. This challenge presents in two major areas: 1) processing of data from on-board sensors, and; 2) processing of data for autonomous-control functions such as docking, landing, and roving. In both areas, mission demands for space computers are rapidly increasing, while conventional on-board computing technologies are falling behind, in terms of the high performance required in harsh space environments with limited size, weight, and power, as well as the inherent hazards of radiation effects beyond our planet's atmosphere.



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In 2015, CHREC researchers achieved a major milestone in basic and applied research for spacecraft computing with the development and technology transfer to center members of the new CHREC Space Processor (CSP). The CHREC CSP is a novel form of hybrid, reconfigurable space computer that can achieve an unprecedented mix of high performance and reliability with low power, size, weight, and cost. As of December 2015, 14 new space missions (a technology pallet for the International Space Station, a space-science satellite, and 12 weather satellites) have adopted CSP. These have been scheduled for launch into Earth orbit in 2016 and 2017 for NASA and PlanetiQ (both are center members), equipped with a total of 39 CSP computers. Moreover, these and other CHREC members are evaluating CSP for additional missions.

The primary challenge with space electronics is how to prevent or at least mitigate the harmful effects of solar and cosmic radiation on electronics. Some devices feature radiation hardening in fabrication by process and design. This approach can usually minimize radiation effects on electronics; but not without trade-offs. Radiation hardening can result in lowered performance and larger sizes, weights, power consumption, and cost. These are due to the nature of the hardening process. Other devices, such as those used in consumer laptops, tablets, smart phones, etc., achieve high performance with lower sizes, weights, power consumption, and cost, but many of these technologies suffer from poor to no reliability when subjected to space radiation.

CSP features a novel, hybrid combination of higher-grade commercial devices (e.g., main processors and memory units) where performance is critical, and radiation-hardened parts (e.g., flash memory, watchdog controller, power and reset circuits) when reliability is critical. These can then be supplemented by a myriad of techniques (e.g., replicated bootstraps and configurations with RSA authentication, internal and external watchdog units, error-correcting memory units, and configuration memory scrubbing from the field of fault-tolerant computing). In this manner, CSP offers an innovative solution for space computing that is faster, lower size, lower weight, lower power, and less cost than fully hardened computers, while being more reliable than fully commercial computers.

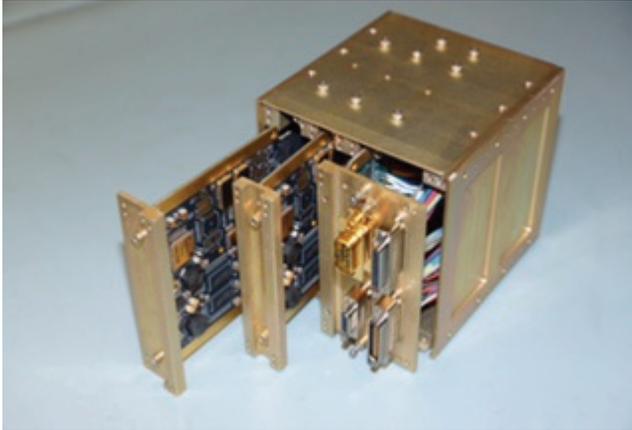
CSP also features an innovative, reconfigurable, central processor, an FPGA SoC (i.e., field-programmable gate array, system on chip) known as the Xilinx Zynq. The Zynq in CSP contains a multicore CPU (twin ARM Cortex-A9 cores with Neon accelerators) able to execute (thanks to CHREC) flight software systems (e.g., core flight system or CFS from NASA Goddard) atop any one of several operating systems (e.g., Linux, RTEMS, Wind River's VxWorks). The Zynq also contains a potent, reconfigurable logic array that can be configured either on the ground or in flight to match the unique needs of each mission, application, instrument, etc., for faster speed and lower power.

Economic impact: The hybrid and reconfigurable approach of CSP is proving its potential to dramatically increase capabilities and reduce costs associated with spacecraft and space-based computing. The breakthrough could lead to significant economic impacts in the U.S. space industry. In terms of direct economic impact, instead of having to develop new, hardened processor technologies (at an estimated cost of \$20M+ for each new processor) and then exclusively rely upon these expensive (e.g., \$10K to \$100K per device) and slower devices for reliable space systems, the CSP approach enables future systems to more reliably achieve higher performance at lower cost and do so with less size, weight, and power. Moreover, with this approach, the space industry can rapidly exploit technology breakthroughs from the consumer marketplace as new devices emerge. The indirect economic impact here may even be more significant. New space missions may be made more feasible when this novel approach is used. Major savings may come from spacecraft and launch vehicles that are smaller and less expensive than would otherwise be the

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case, resulting in scientific discoveries and economic benefits that otherwise might not have been realized.

For more information, contact Alan George, 352-392-5225, george@hcs.ufl.edu, Bio <https://www.ece.ufl.edu/users/george-alan-d>



CSP is a novel form of hybrid, reconfigurable space computer that can achieve an unprecedented mix of high performance and reliability with low power, size, weight, and cost.

