Center for Electromagnetic Compatibility (CEMC)

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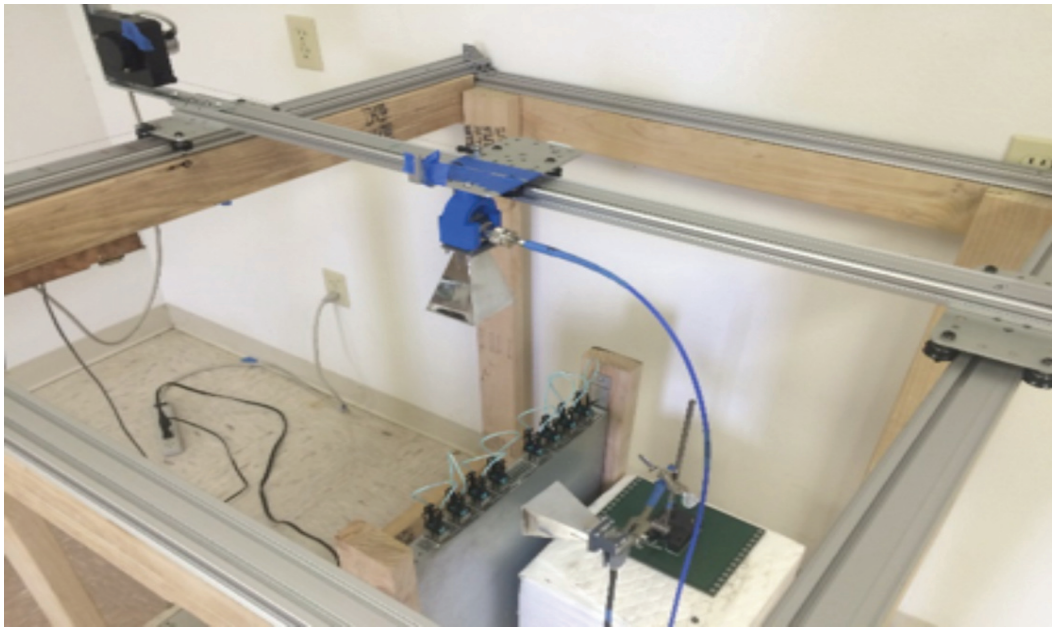
Sparse Emission Source Microscopy (ESM) Scanner with Super-Resolution Capabilities

Localization and identification of electromagnetic interference (EMI) sources is a major problem of electromagnetic compatibility (EMC). High-speed electronic devices produce Emission Source Microscopy (EMI) in a wide frequency range. This is due to multiple radiation coupling paths that involve structures such as cables, heat sinks, connectors, enclosure slots, ventilation openings, etc. Traditional EMI source localization techniques such as near-field scanning often produce ambiguous results that do not adequately identify and quantify the sources and coupling paths.



Set-up of an emission source microscopy (ESM) scanning a device under test (DUT)

This breakthrough's sparse emission source microscopy scanning provides a method for quick and robust localization of the EMI sources along with an estimate of the radiated power of each source. The measurements are performed by recording the field magnitude and phase on the plane above the device under test (DUT) as shown in Fig. 1, and by applying a focusing algorithm to obtain the microwave image of the radiating sources as shown in Fig. 2. A probing antenna is located at a distance of several wavelengths from

the DUT. This makes for optimal receiving antennas. Manual scanning, together with the real-time imaging, allows adaptation of the scanning strategy to the particular type of the DUT. It only scans in areas relevant to an EMI coupling path under scrutiny. This dramatically decreases scanning time; from hours in traditional scanning methodologies to minutes in the current approach.

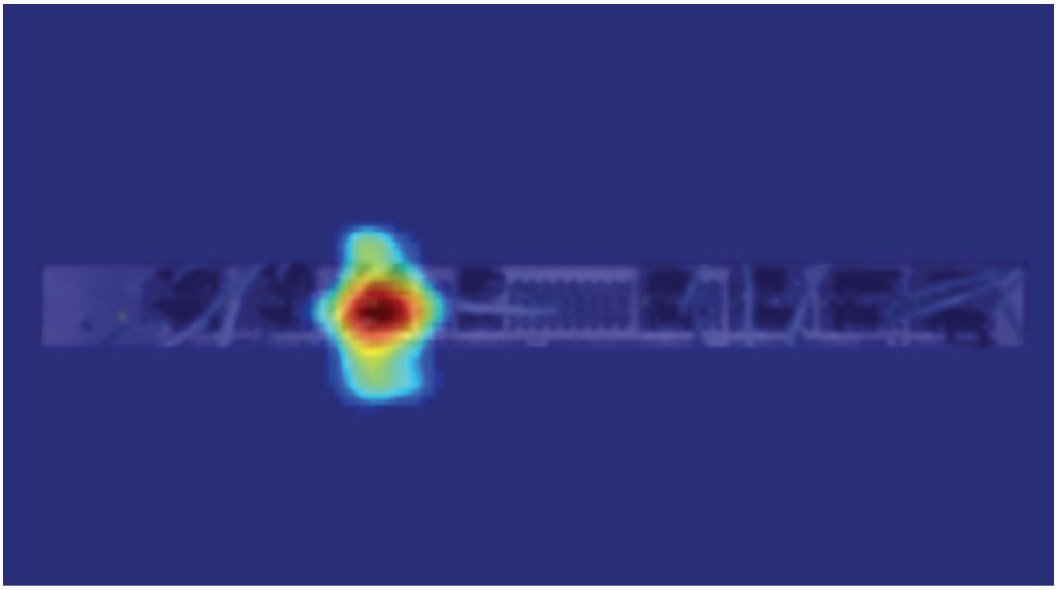


Image of the radiated sources at 10.3125 GHz using the ESM scanner

To improve the resolution of the scanner, a water immersion technique is used. This is analogous to liquid immersion in optical microscopy. In water immersion scanning, a plastic tank is placed underneath the scanner frame and filled with water such that the probing antenna is completely immersed. The DUT is placed underneath the tank to avoid contact of the liquid with the electronics. Due to the high permittivity of water in the lower GHz frequency range (around 90 at 1 GHz), and, hence, a short wavelength, resolution is significantly improved; reaching 2.5 cm at 1 GHz. This is a 6-fold improvement over scan in air, allowing resolution of individual components on typical printed circuit boards.

Economic impact: There is a growing market for EMC field scanners; however, most of the scanners on the market are expensive robotic models with prices starting from tens of thousands of dollars. The sparse ESM scanner developed by the CEMC provides an inexpensive alternative with a cost under $2000, not including the vector network analyzer receiver. The ability to generate EMI source and coupling path images within several minutes makes the scanners a unique tool allowing EMC engineers to more timely locate EMI sources with higher accuracy and confidence at the prototyping stage. This lowers the risk of EMI compliance problems late in design cycles. It can be applied to diagnostics for quick fixes of existing problems. Estimating the radiated power of identified sources with ESM avoids time-consuming trial-and-error in anechoic chambers to achieve compliance. Application of the sparse ESM scanner in the EMC design process can signif-

icantly reduce engineering time and the costly EMI retrofits required to achieve EMI regulatory compliance.

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Fixture De-embedding for High-Speed Interconnect Characterization

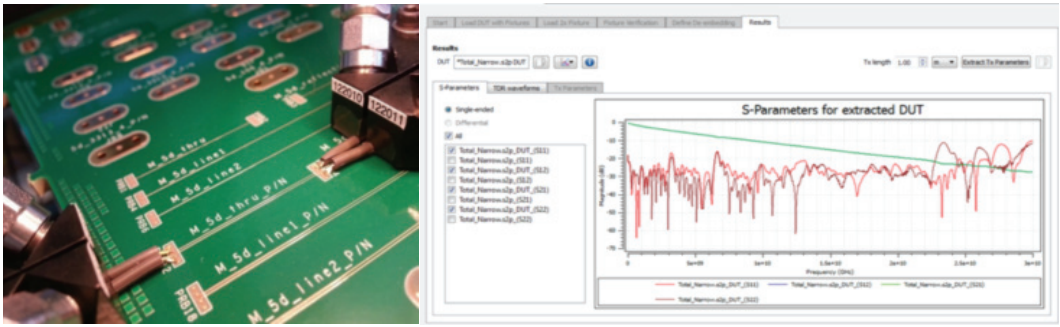
Modern computer systems use high speed differential serial links as input/output (I/O) interfaces, such as USB, PCI-Express, SATA, etc. The data rate of differential serial links has grown exponentially over the last two decades to meet ever-increasing bandwidth requirements. When USB1.1 was introduced at 1998, it was running at 12 Mbps. Fast-forward to today, USB3.1 is running at 10 Gb/s, almost 1000 times faster than USB1.1. With increasingly fast data rates, signals propagating in the printed circuit board (PCB) degrade significantly due to the non-ideal effects such as copper surface roughness, the fiber-weave effect, dielectric dispersion, noise interference, etc. In other words, the signal propagation path in the PCB needs to be characterized and designed properly, otherwise high speed signals cannot propagate with enough fidelity and errors can then occur.

Measuring PCB structures is challenging, especially at high frequencies. The main reason is that test fixtures are necessary to connect the PCB structure under measurement to the measurement instrument. At high frequencies, the effects of the test fixtures become significant enough so that the measured results do not reflect the actual behaviors of the PCB structure. To remove the effects of the test fixtures, some methodologies such as TRL (thru-reflect-line) and LRM (line-reflect-match) were developed. These error-correction methods require several calibration patterns with different loadings. The calibration patterns need to be constructed in the same PCB as the PCB structure under measurement, which occupy a large amount of board area. The resulting error correction procedure can be cumbersome, involving several additional measurements. It demands uniformity among the calibration patterns that are difficult to achieve due to manufacturing variations.

To address the challenge, CEMC researchers developed a new type of de-embedding methodology. The breakthrough de-embedding approach uses only one 2X-Thru pattern, as compared to six patterns needed for the TRL calibration to cover the frequencies up to 50 GHz. In this new approach, the S-parameters of the 2X-thru structure are measured first. Assuming the 2X-Thru structure is approximately symmetric, the S-parameters of a 1X structure can be calculated directly from the 2X-Thru measurement. Once the S-parameters of the 1X structure on both sides on the DUT are obtained, the S-parameters of the DUT can be readily calculated. This significantly simplifies calibration/de-embedding procedures as compared to the traditional TRL calibration where six calibration structures are typically needed. An engineering tool has been further developed to help the industry address this design challenge.

This work represents a significant improvement over the previous state of the art because the new methodology tool: 1) fits well with "real-world" engineering practice and does not require that users understand the electromagnetics, algorithms and mathematics; 2) significantly simplifies the calibration pattern designs and measurement procedures, and reduces measurement time; and, 3) are flexible enough and sufficiently effective to handle the complex real-world structures that are necessary to characterize high-

speed interconnects. Combined with different probe designs, they can be used for applications ranging from laboratory measurements to product-line testing.



(Left) A differential printed circuit board trace is measured using micro-probing station. To characterize the electrical performance of the trace only, the effects of the probes and the probe pads need to be eliminated from the measured results. (Right) A screenshot of the developed engineering tool.

Another significant contribution from Center for Electromagnetic Compatibility (CEMC) is de-embedding sensitivity analysis. De-embedding practices among current industry tools are following a brute-force approach, wherein results are generated by the tool without error checking. In-depth de-embedding analysis are then performed by the CEMC research team to reveal the mathematical relationships between de-embedding errors versus the quality of fixture designs. This breakthrough helps users to understand how good the de-embedded results are and significantly reduces the possibility of unknowingly using data beyond valid frequencies.

> **Economic impact**: The developed engineering tool has been used in several CEMC member companies including Intel, Cisco, and IBM. The cost reduction alone generated by using the tool instead of alternative commercial software is estimated to be at least $100K a year among these companies. Further, the innovative methodology significantly reduces costs of fabricating complex calibration patterns. It significantly shortens the measurement time from a couple hours for one DUT to less than 30 minutes and is much less prone to error. The associated cost savings are estimated to be at least $2M/year at this stage for these companies. The tool can also be extend to other interconnects beyond PCB (such as connector, cabling, etc.), which can further increase the economic impacts.

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