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A 5–10 GHz SiGe BiCMOS FPGA with new configurable logic block

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Abstract

This paper presents a new multiplexer based FPGA, which can operate at a clock frequency of 5–10 GHz. Redundant switches on the original signal paths are removed improving the performance. The configurable logic blocks (CLBs) power is greatly reduced by using a revised multiplexer structure and turning off unused cells dynamically. More routing capabilities are provided with more inputs/outputs in each direction than similar designs. A chip consisting of four FPGA ring oscillators was fabricated. The Spice simulation results and chip measurements are presented.

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Keywords: Field programmable gate array; Gate-array; High-performance; Low-power-design; SiGe; Programmable logic array; Reconfigurable-system; Current mode logic

1. Introduction

The field programmable gate array (FPGA) consists of an array of configurable logic blocks (CLBs). The user programmable feature of an FPGA makes ASIC design easy and decreases time-to-market. Compared to traditional programmable logic devices (PLDs), FPGAs' configurable logic blocks provide many more functions than PLDs. Different kinds of logic blocks of FPGAs have been studied thoroughly [8]. As shown in [8], a multiplexer based FPGA has better performance than LUT, NAND and AND-OR based FPGAs. One multiplexer based FPGA, the Xilinx XC6200 [4,10], has fallen from favor due to its poor routing capability. This paper brightens the future of multiplexer based FPGAs by converting conventional CMOS multiplexers to BiCMOS multiplexers. A new structure is presented greatly increasing the routing capability. The number of switches on the signal paths is reduced to reduce power and increase performance. With the IBM SiGe 7HP BiCMOS

technology, a measured gate delay of 100 ps is presented in this paper.

A power saving method is utilized to overcome the disadvantage of current mode logic circuits. Unused multiplexers will be turned off to save power. Some new schemes for multiplexers are also provided to save power. The proposed power is less than 10 W with heavily pipelined applications for a 20×20 gate array.

The layout of this paper is as follows: Section 2 briefly describes the IBM SiGe BiCMOS 7HP technology and Section 3 presents the structure of this new FPGA. It also introduces a new multiplexer structure, which is used in the design, and a power-saving method that dynamically turns off unused circuits. Section 4 presents circuit simulation and experimental results. Section 5 summarizes the present work and discusses relevant future developments.

2. IBM SiGe BiCMOS 7HP technology

This FPGA design is implemented using the IBM SiGe BiCMOS 7HP technology. The technology has all features of Si-base transistors, such as polysilicon base contacts, polysilicon emitter contacts, self-alignment and deep-trench isolation. A linearly graded Ge concentration profile in

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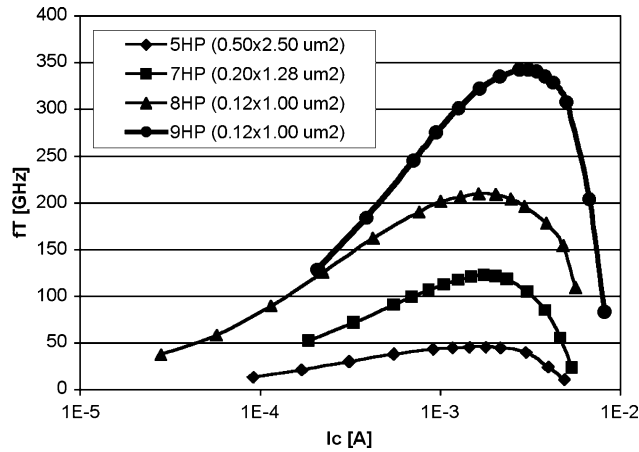


Fig. 1. I_C versus f_T in the four generations of IBM High Performance SiGe BiCMOS process. I_C value for peak f_T is at 0.9 mA.

the base region dramatically increases the transistor's performance, such as current gain, early voltage and base transit time [5,6,9]. Fig. 1 shows an I_C and f_T curve in the four generations of IBM High Performance SiGe BiCMOS technology. The peak f_T point of the smallest NPN transistor in 7HP is at 1 mA. Using less current in the collector causes more gate delay in circuits while less power is used. The high-speed 7HP circuits introduced later use 1 mA as the collector current.

3. New FPGA structure

3.1. New CLB structure

A multiplexer based FPGA has been of interest for a long time. Several attempts have been made to increase the speed and routing capability. One gigahertz-FPGA was reported in Ref. [7]. However, limited routing capability and high power usage prevent it from being widely used. A better performing FPGA is highly desirable.

A single 2:1 multiplexer can provide any two-variable logic function [10]. Table 1 shows sample configurations for inverter, AND and XOR functions. The corresponding configurations can be found in Fig. 2.

All multiplexer based FPGAs apply this feature of 2:1 multiplexers [7]. Some designs use a 4:1 multiplexer and others use MuxA [10]. Fig. 3 shows a proposed CLB using a 2:1 multiplexer. The 2:1 multiplexer is the core of the function block. It generates combinational logic results

Table 1
Example of logic function table

Function	X1	X2	X3
INV	XX	A0	A0
A1 AND B1	A1	B1	A1
A1 XOR B1	A1	B0	B1

XX, Don't care. '1' is for signal. '0' is for complement signal.

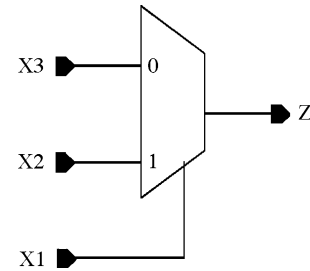


Fig. 2. 2:1 Multiplexer to implement any two-variable logic function.

(FZ). Sequential logic results (SZ) can be implemented with a master-slave latch (MS-Latch) and a feedback signal (FD) from the MS-Latch back to the input selecting multiplexers. All logic results are sent out to four neighbor cells: north, south, west and east. More routing capabilities are provided by redirecting signals in one direction to another (RW, RE, RS and RN) and a shared bus, FastLANE, which connects four CLBs in the same row or column. The outputs in each direction of a CLB consist of a combinational logic result, a sequential logic result and a redirection signal. The inputs in each direction of a CLB consist of one combinational logic result from a neighbor cell, one sequential logic result from a neighbor cell, one redirection signal and one FastLANE. Three multiplexers select three signals from a total of 16 or 17 inputs and feed them into the core multiplexer. The combinational function of a CLB is determined by the configuration of those input multiplexers (two 17:1 multiplexers and one 16:1 multiplexer).

The inputs of the redirection multiplexers are the inputs of the CLB without FastLANEs and the signal from same direction. For example, the redirection multiplexer facing east does not have the input from east side since getting one signal and routing it back in the same direction wastes routing resources. Comparing this CLB structure with the XC6200 and other multiplexer-based FPGAs [6,10], one can see that the new structure has reduced the gate delay from seven gates to four gates. The new structure does not have CS, PR and 4:1 output multiplexers but still provides more routing capability. For example, one can route the function result to the east neighbor and the south redirection signal to the east simultaneously.

The gate delay of a single level 16:1 multiplexer is larger than a two-level 16:1 multiplexer as shown in Fig. 4 due to high loading. The first level inputs consist of the 16 inputs in four directions. The second level then selects one output from the first level to finish the 16:1 multiplexing function. For the 17:1 multiplexer, the second level multiplexer is implemented with one more input from the feedback signal. The 5:1 multiplexer in the second level will be explained later.

3.2. New multiplexer design

Besides the new CLB, new multiplexers are used in the design. There are two kinds of traditional multiplexers.

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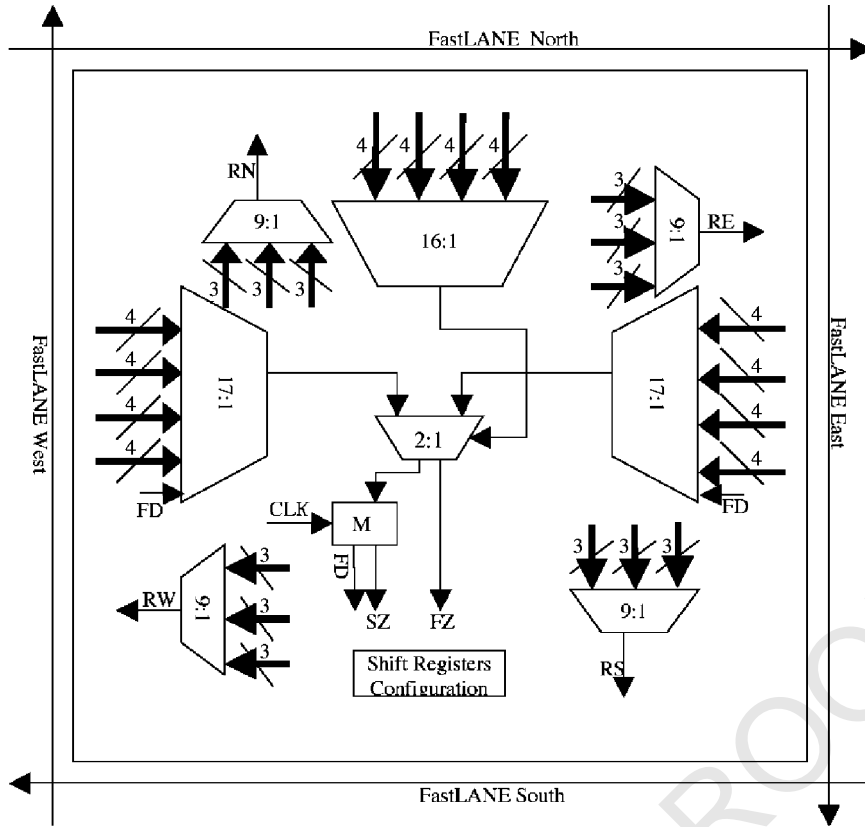


Fig. 3. New CLB Structure. Combinational and sequential logic results are sent directly to neighbor cells, thus reducing gate delay from 7 to 5 gates.

One kind of traditional BiCMOS 4:1 multiplexer is shown in Fig. 5. The two-level selection tree of S1, S2 acts as a decoder. Only one BJT pair is selected at a time, permitting the desired signal to pass through. An 8:1 multiplexer can be built with the same style but with a taller current tree. A taller current tree requires a higher voltage supply, which increases total power. Another kind of multiplexer is a bipolar multiplexer similar to the one in the Fig. 5 except the NMOS transistors are replaced by bipolar transistors. The bipolar multiplexer requires a higher voltage supply but has a faster switching speed. In an FPGA design, routing multiplexers only switch during application loading; therefore, the switching speed is not a critical issue.

Fig. 6 shows a new 4:1 multiplexer. An additional decoder is needed to select pass-through signals. After configuration, the decoder only permits one select

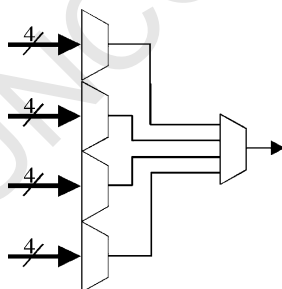


Fig. 4. 16:1 Multiplexer utilizing two level multiplexing.

bit (S0–S3) to be set. Thus, the corresponding BJT pair is turned on to pass signals through. The decoder can be implemented with CMOS to save power and space. The new multiplexer structure has three advantages:

1. All multiplexers become single-high multiplexers, which do not require a higher supply voltage. A 16:1 multiplexer uses the same voltage supply as a 2:1 multiplexer.
2. By resetting all select bits, a multiplexer can be turned off, whereas a traditional multiplexer must always have one current branch on.

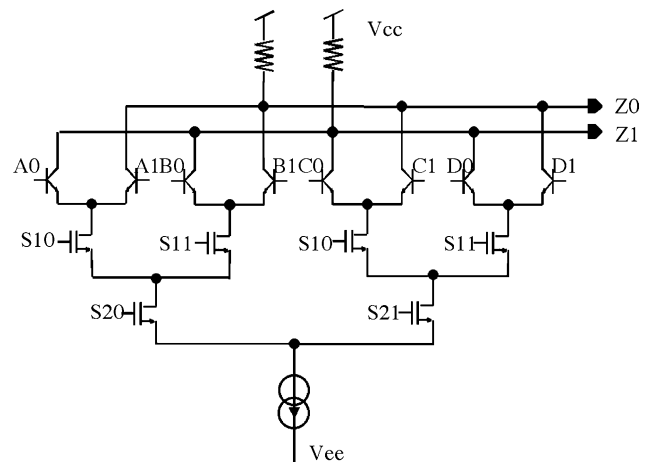


Fig. 5. Traditional 4:1 multiplexer using a two-level current tree selection.

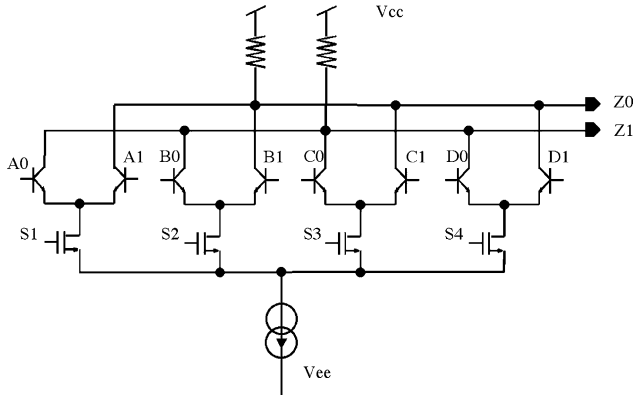


Fig. 6. New 4:1 multiplexer using single-level current tree selection.

3. In a traditional design, multiplexers have 2-to-*n* inputs since select signals are differential. In the new design, one can implement a multiplexer with any number of inputs, such as 9:1 multiplexers and 17:1 multiplexers as are required in Fig. 3.

3.3. Multi-mode routing

Turning off unused circuits is a common scheme to save power. In this FPGA design, the method is realized dynamically by the loaded user applications. At the chip level, unused CLB's will be turned off to save power. In this design, a Master-Key signal indicates a **Mute Mode** for the CLB array. An application using one CLB has a configuration pattern to turn off the other 399 CLB's in a 20×20 gate array.

In a single CLB, there are also unused multiplexers and output drivers when an application is loaded. Turning off those circuits saves more power. At the CLB level, the dynamic routing will be completed as follows: (Output drivers configuration depends on neighbor cell requirements. It is not listed here.)

1. *Normal mode*: when a CLB only uses its combination logic function, the sequential logic circuit (MS-Latch) and all redirection multiplexers may be turned off to save power. Besides sequential logic circuits, more circuits can be turned off in the normal mode. Each CLB needs two signals to generate a logic function. Therefore, at least two output-drivers or two redirection multiplexers in its neighbor cells may be turned off to save power.
2. *Sequential mode*: a CLB performs a sequential logic function. The core multiplexer and MS-Latch is turned on. Redirection operation is off.
3. *FastLANE mode*: if input signals of a cell are selected from the FastLANE, all four output-drivers in all neighbor cells may be turned off to save power.
4. *Redirection mode*: when one cell is configured to redirect a signal from one neighbor cell to another neighbor cell, only the redirection multiplexer needs to be turned on.

Table 2
Dynamic routing configuration

Design	Core	Latch	Inputs	Redir.	Trees
Mute mode	OFF	OFF	OFF	OFF	0
Normal mode	ON	ON	XX	OFF	9
Sequential mode	ON	ON	XX	OFF	11
FastLANE mode	ON	XX	OFF	OFF	3
Redirection mode	OFF	OFF	OFF	ON	3/6/9/12
Full mode	ON	ON	ON/XX	ON/XX	21

XX, depends on neighbor cell configuration.

Other circuits in the CLB may be turned off to save power.

5. *Full mode*: full mode is a very rare situation in an application. When a CLB performs sequential logic and also redirects three signals, the CLB works in Full Mode. All current trees are turned on. (No application can configure all CLB's into Full Mode in a gate array).

With the new features of the multiplexers, decoders of multiplexers may be turned off in order to turn off unused input circuits. Table 2 shows a power estimation of dynamic routing.

3.4. Memory structure

A memory configuration structure is used to store user applications and to supply configuration bits to multiplexers. In the previous design, 26 memory bits were used to configure a single cell. A parallel memory configuration structure was used. Memory bits were supplied by a 26-bit wide ribbon cable. In this new design, 41 memory bits are needed to configure a cell. Due to the large number of configuration bits, the parallel configuration is inefficient. Therefore, a shifted register configured memory structure is used to configure memories.

Fig. 7 shows a shift register configured memory configuration structure. Two memory banks are utilized in this design to implement the FPGA with two personalities. Each personality might load one application at a time. The two banks' enable signals are used to switch between personalities. One clock signal is used to shift memory data. The memory banks' enable, data and clock signal are system signals routed to every single cell in a gate array.

3.5. Overall performance

The layout and component list of this newly designed basic cell structure are shown in Table 3 and Fig. 8. A single basic cell layout is approximately 180 by 200 μm² with memory configuration structures.

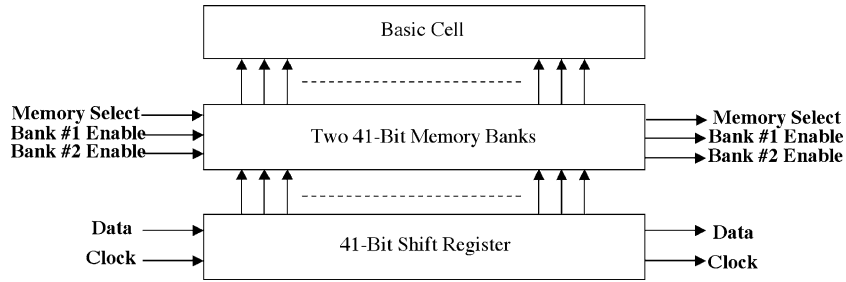


Fig. 7. Shift registers configure memory banks. Data, clock and memory banks' enable signals are system wide.

The new structure has several advantages over similar designs [2]. Instead of sending only one output to a neighbor cell in one direction, the new structure sends out three outputs to a neighbor cell in one direction.

The first advantage is the improved routing capability. One of the examples is shown in Fig. 9. C5's logic function result is required by C7, but C6 also has a logic function result required by C7. In the old CLB, routing is forced to go from C1–C2, from C2–C3 and then from C3–C7. In the new CLB, routing can be taken through C6 since both a logic function result and a redirection function can be routed east.

The second advantage over the previous design is its better performance. The new structure has only two multiplexers on the input paths of the core 2:1 multiplexer. There are no switches or multiplexers on the output paths. Switches on signal paths are minimized to provide the best performance that a multiplexer based FPGA can have. There are only three gate delays through a CLB and there are no interconnect switches. This is why multiplexer based FPGAs perform better than other FPGA structures.

Another advantage of this new design is the reduced power consumption. The power usage of the full FPGA chip is reduced. A lower voltage supply is possible due to the use of single high multiplexer CML trees. Unused CLBs and circuits are turned off as needed by individual loaded applications. Power can be further reduced by supplying less current in each CML current tree with a trade-off of performance. A power and delay table is presented for comparison with similar designs. Fig. 10 and Table 4 show a power and performance trade-off diagram.

3.6. Testing plan

The final goal of this project is to design a 48×48 or large gate array with clock frequency from 5 to 20 GHz. The project has the following testing strategy:

1. Single cell test: one single cell chip was fabricated in 2000 to test the functionality, BiCMOS multiplexer design, chip's performance and the memory structure. The testing results are presented in [2].
2. Power and performance test: once functionality, the BiCMOS multiplexers and the memory structure were tested, a chip containing more cells will be tested for

lower power and higher performance ideas. The chip, including ring-oscillators, is fabricated with the IBM 7HP BiCMOS technology. The testing results are detailed in Section 3.7.

Table 3
Chip component list

Label	Component
A	West redirection multiplexer
B	South redirection multiplexer
C	17:1 Multiplexer
D	17:1 Multiplexer
E	16:1 Multiplexer
F	North redirection multiplexer
G	East redirection multiplexer
H	2:1 multiplexer and drivers
I	Output drivers
J	Master-Slave latch
K	Memory configure system

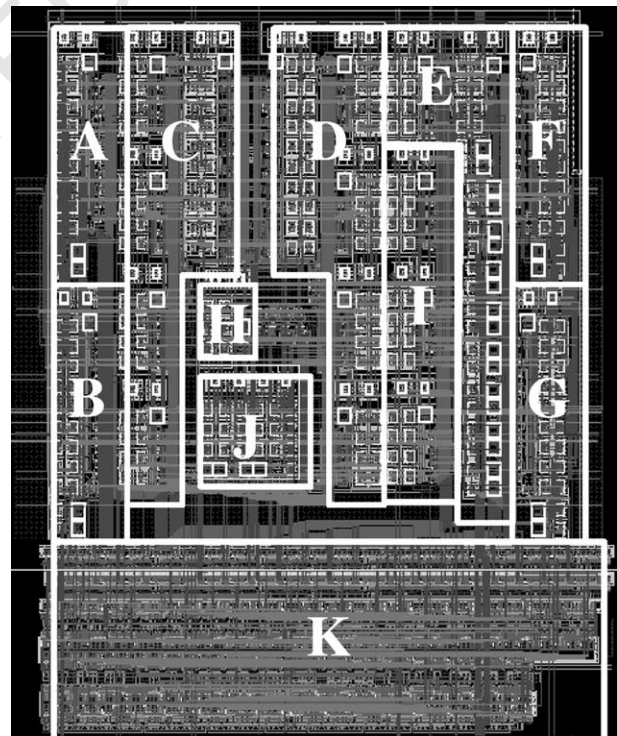


Fig. 8. Basic cell layout. The size of a single cell is 178×203 μm². The corresponding list is in Table 3.

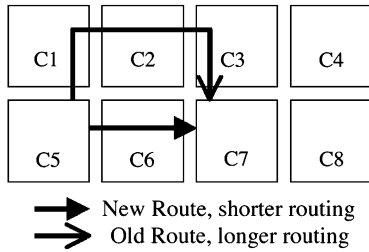


Fig. 9. Comparison between two routing method. New basic cell structure has obvious advantages over the old cell structure.

3. Scalable gate array test: when the single cell performances and power consumption met scalable criteria, i.e. low power, high-speed, good routing capability, etc. a larger gate array was implemented. Due to space limitations, only a 20×20 gate array was submitted for fabrication with the IBM 7HP BiCMOS process in July 2003.

The testing plan is simulated with IBM SiGe 7HP models. The models have been updated several times since it's first released. Most parameters of the models agree with measurement with little deviation. As shown in later part of this paper, the maximum difference between simulation and physical measurement is 15%. Therefore, the simulated results can partially be used as evidence of circuits' performance.

3.7. 20×20 Gate array

The 20×20 gate array is an important milestone in the project. Two important issues in this chip are clock distribution and system wide memory configuration.

Clock tree distribution is implemented by an H-Pattern. To save power on the clock trees, a multi-mode routing idea is deployed as shown in Fig. 11. Each high-speed clock driver has an enable bits to turn it on/off. Since the MS-Latch is the only circuit in a cell that needs clock signal,

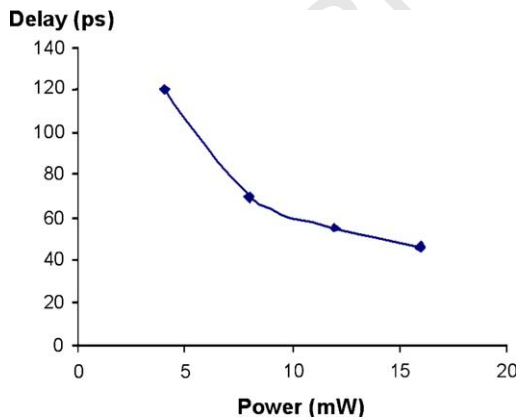


Fig. 10. FPGA Power-Delay trade-off in the IBM 7HP BiCMOS technology.

Table 4 Power and delay chart for various FPGA designs

Design	Current (mA)	Power (mW)	Delay (ps)
Similar structure [2]	0.6	53	80
New structure	0.8	16	46
	0.6	12	55
	0.4	8	70
	0.2	4	120

An AND gate is simulated for design comparison. Similar structure does not have the dynamic routing feature.

the MS-Latch's control bit might be used to turn on/off the clock drivers. The second level clock driver enable bits are controlled by the first level drivers. Upper level clock drivers use the same scheme. If one MS-Latch requires a clock, the cell will turn on all the clock drivers on the path to reach the clock source. Otherwise, the MS-Latch votes to turn off clock drivers to save power. Such a clock distribution scheme guarantees the clock signal reaches each cells without clock skew and delivers the clock signal to the cells needing it. No clock drivers' power and dynamic power is wasted.

The system wide memory configuration structure is consistent with the single cell memory configuration structure. Fig. 12 shows the system wide structure. As described previously, a cell's memory configuration structure uses the serial input of shift registers to provide parallel inputs to the memories. Each cell's input and output might be connected as follows to provide system wide distribution.

The following Fig. 12 shows a 5×5 mm², 20×20 gate array layout that has been submitted for fabrication. The input pads include input drivers for memory configuration, external system clock, and external inputs. The output pads include output drivers for memory configuration output for verification purpose, and outputs from the FPGA. System clock is provided by an on-chip VCO and external system clock. A user can specify which clock he wants to use via a high-speed 2:1 multiplexer.

In the 7-metal layer IBM 7HP BiCMOS technology, the first three metal layers are used for cell interconnection. Two metal layers are used for clock distribution. Two metal layers are used to supply power.

4. Circuit simulation and chip measurement results

An FGPA can load various applications to prove its functionality and performance. In this paper, a clock divider circuit and a demultiplexer is simulated to test speed and functionality (Fig. 13).

A clock divider is a very simple circuit to find the maximum operation frequency of a circuit. A circuit is shown in Fig. 14, a buffer is implemented in the basic cell and supplies data to the Master-Slave Latch. If the input

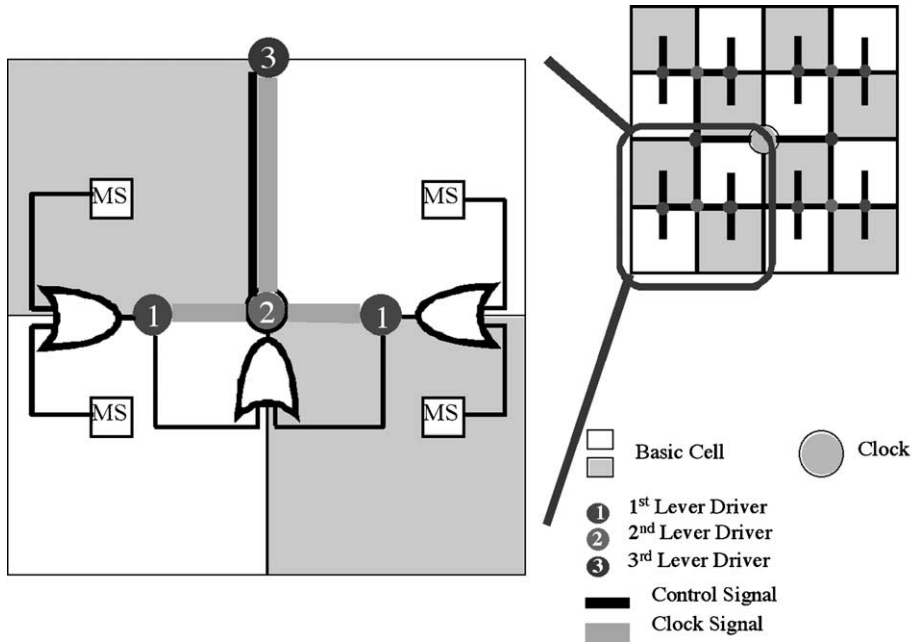


Fig. 11. Clock H-Pattern distribution with dynamic clock control. Level-one driver’s enable bit will disable level-two if level-one driver is not used.

clock is less than the maximum operation frequency, the circuit will operate correctly by outputting half the frequency of the input clock. Otherwise, the output data will be invalid. Fig. 15A and B show a simulation result of the clock divider. In Fig. 15A, the input clock has a frequency of 10 GHz and the output shows a 5 GHz clock signal. In Fig. 15B, the input clock has a frequency of 13.5 GHz and the output shows several invalid voltages, which indicate that the clock frequency has exceeded circuit capability.

A demultiplexer is used in serial–deserial circuits to decode and distribute a transmission channel to different

channels. Fig. 16 shows a sampling single cell circuit used in the demultiplexer. The DATA is connected to the transmission channel. The SEL is connected to a 4-bit barrel counter, which has half the clock frequency of the system clock. In a 1:16 demultiplexer, 16 sampling cells will be connected in parallel. The barrel counter will enable one SEL at a time and shift to the next sample cell

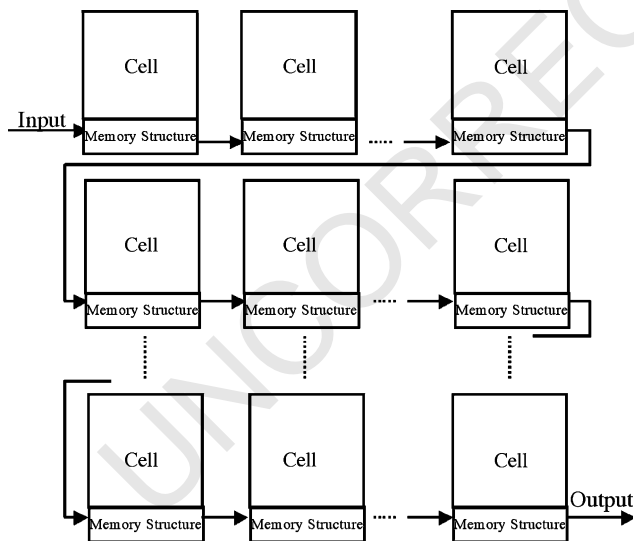


Fig. 12. System wide memory configuration structure. Memory configuration inputs are serially connecting to each cell. The simulation memory configuration load-time is 4 ms for 20×20 gate array.

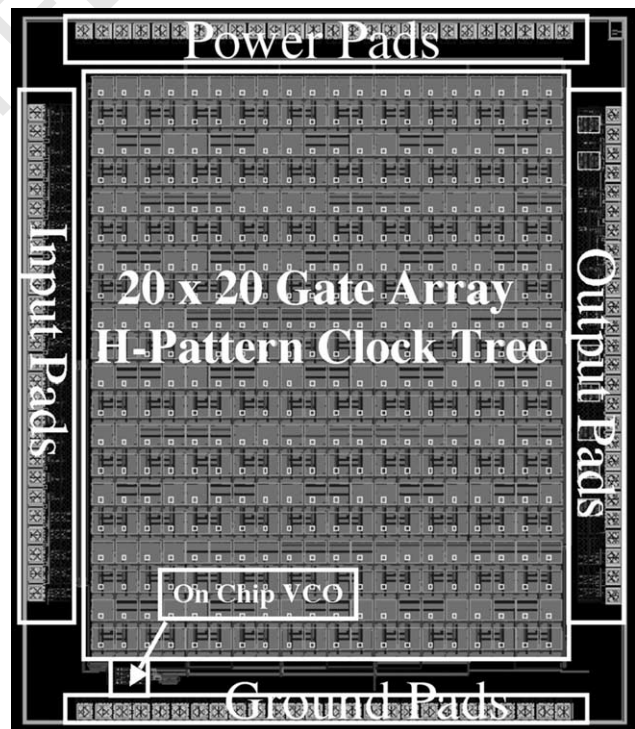


Fig. 13. Submitted 20×20 gate array chip. Chip size 5×5 mm².

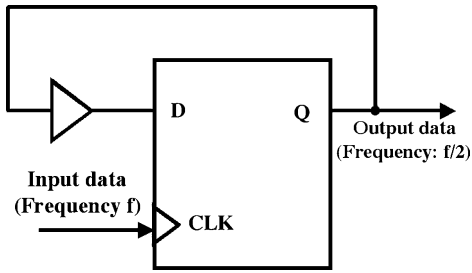


Fig. 14. Clock divider to obtain maximum operation frequency.

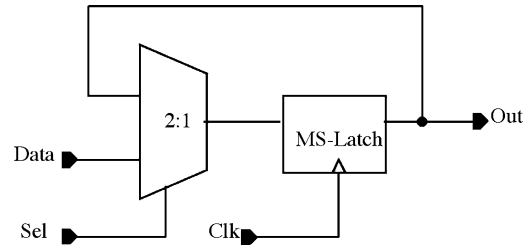


Fig. 16. Demultiplexer sampling circuit.

after one clock cycle. When the SEL is enabled, the DATA will be latched in the MS-latch. When the SEL is disabled, the DATA will be held at the MS-latch by selecting the feedback. If needed, another pipelined buffer circuit can follow the output and hold the result. Fig. 17 shows a simulation result with a 10 GHz system clock.

The new multiplexer based FPGA has shorter gate delays, reduced power usage and more routing capability than similar multiplexer based FPGA designs. To demonstrate the advantages of the new FPGA structure, a chip was fabricated in June 2002. This test chip utilizes IBM's SiGe BiCMOS 7HP technology. Four hardware configured

FPGA ring oscillators are built to demonstrate the performance in a $2 \times 2 \text{ mm}^2$ area. The layout of the chip is shown in Fig. 18.

The two left ring oscillators in Fig. 18 (A and B) are high speed FPGAs with gate delay of 100 ps. The left bottom oscillator has diodes on the current tree to prevent collector-emitter breakdown. The two right ring oscillators (C and D) are low power FPGAs with gate delay of 250 ps. The right bottom oscillator also has diodes on the current trees to prevent collector-emitter breakdown. A waveform of the high-speed ring oscillator is shown in Fig. 19. The measurement is taken at 20 °C. The voltage supply is 2.5 V. The output voltage swing is 400 mV.

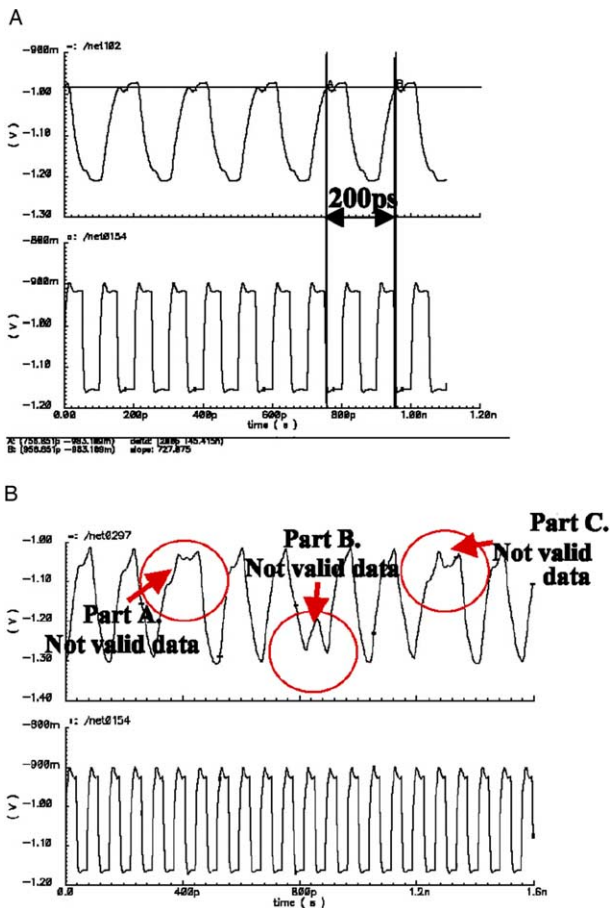


Fig. 15. (A) Simulation of valid clock frequency of 10 GHz. (B) Simulation of 13.5 GHz clock with an invalid data output signal.

4.1. Performance measurement discussion

Spice simulations for the high-speed oscillators show a clock period of 680 ps. The frequency of oscillation is defined by Eq. (1).

$$f = \frac{1}{2 \cdot N \cdot T} \tag{1}$$

where T is the gate delay through the CLB. From our simulation results, each CLB has a gate delay of 85 ps. The measured high-speed oscillator in Fig. 19 shows a clock period of approximately 800 ps, and a CLB gate delay of 100 ps. For the similar designs, the estimated gate delay ranges from 120 to 150 ps at a considerable power consumption. The difference between simulation and measurement is due to wire resistance, parasitic capacitance and circuit parasitic capacitance.

4.2. Power measurement discussion

The chip contains 12 pad drivers, five divide-by-eight circuits, one divide-by-two circuit, two high-speed FPGA ring oscillators, two low-power FPGA ring oscillators and one regular ring oscillator. Pad drivers, divide circuits and high-speed FPGA ring oscillators utilize a 2.5 V power supply. The regular ring oscillator and low-power FPGA ring oscillators utilize a 2.0 V power supply. A 2.5 V power supply feeds the west side of the chip and a 2.0 V power supply feeds the east side of the chip. To power up the high-speed FPGA ring

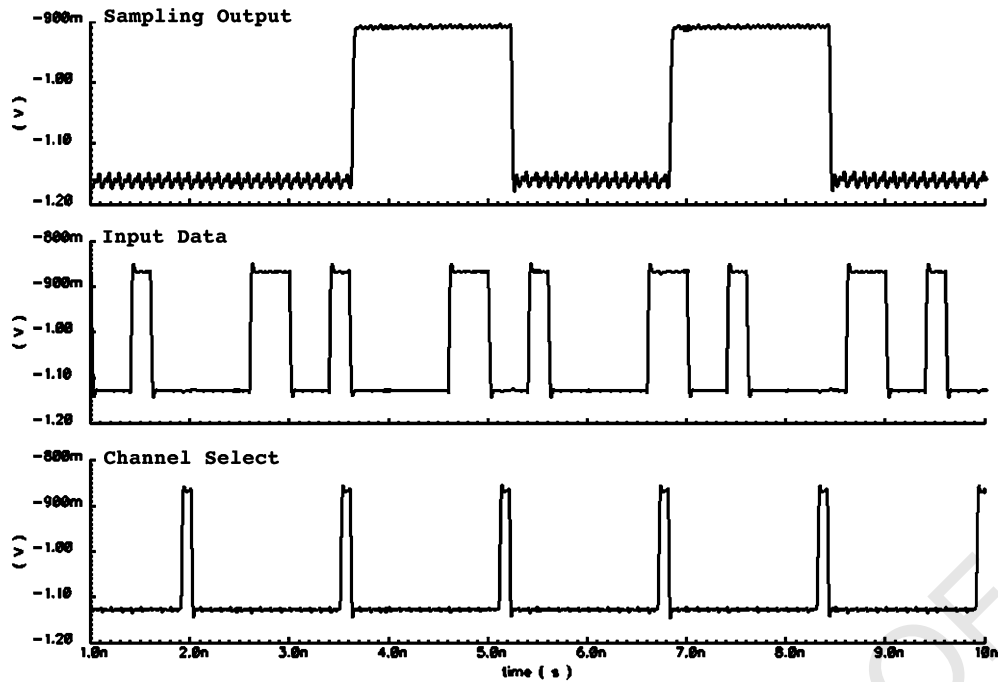


Fig. 17. Simulation results of 1:16 demultiplexer with 10 GHz system clock.

oscillators, the power supply is solely needed on the west side of the chip. To power up the low-power FPGA ring oscillators and CML ring oscillator, a 2.5 V power supply is needed on the west side for all pad drivers and divide circuits and a 2.0 V power supply is needed on the east side. Table 5 shows the designed power consumption of this chip.

For the two high-speed oscillators, the predicted power consumption is 848 mW for a 2.5 V power supply with 339 mA total current. The measured power supply voltage is 2.5 V when the ring oscillator starts to oscillate.

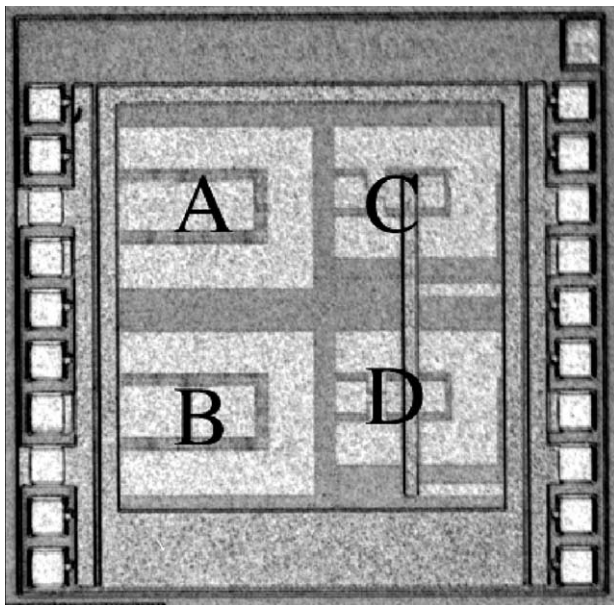


Fig. 18. Microphotograph of the IBM 7HP BiCMOS chip layout. (A) 4-Stage ring oscillator. (B) 4-Stage ring oscillator with diodes on the current trees. (C) 4-Stage low-power ring oscillator. (D) 4-Stage low power ring oscillator with diodes on the current trees. Chip size: $2 \times 2 \text{ mm}^2$.

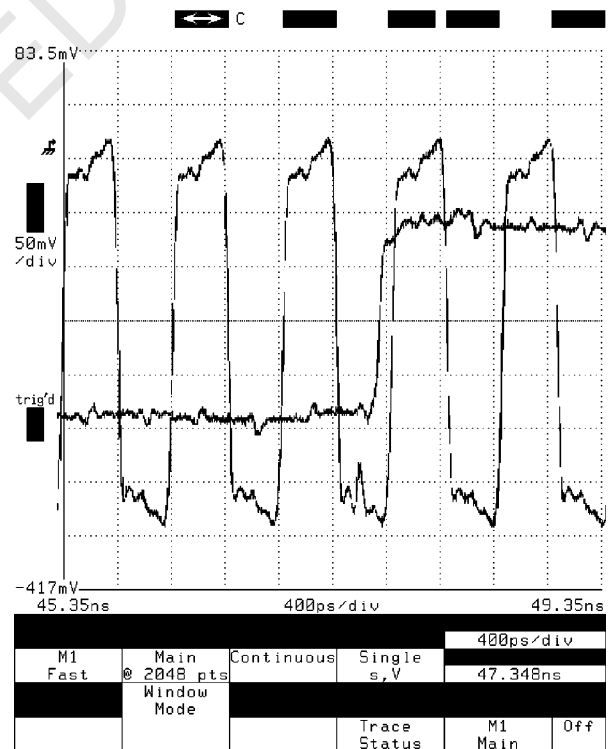


Fig. 19. Chip gate delay measurement screen capture. The high-speed ring oscillator proves a gate delay as short as 100 ps.

Table 5
Current in each fabricated component

Circuit	Current (mA)	Number	Total (mA)
Pad driver	17.00	12	204.00
Divide-by-2	1.23	1	1.23
Divide-by-8	3.69	5	18.45
High-speed RO	57.44	2	114.88
Low-power RO	6.476	2	12.952
CML RO	10.53	1	10

RO stands for ring oscillator.

The measured current ranges from 258 to 295 mA. The reduced current draw is due to the voltage drop over the power rails and resistive losses on the cable.

5. Conclusion and future work

This paper presents a novel multiplexer based FPGA. Compared to a similar previous design, this new design has better performance, lower power usages and better routing capability. Implemented in IBM’s SiGe BiCMOS 7HP technology, the measured gate delay is 100 ps. Power usage is 10 mW per CLB or less.

A larger 20×20 gate array has been shipped for fabrication. The larger gate array will target wider applications with a system clock up to 10 GHz. The power usage is less than 20 W for the entire chip.

Further developments include improving routing capabilities and adding more functionality into the CLB. Routing capabilities can be improved further by routing the FastLANE with the redirection multiplexer. The functionality of the CLB can be improved by adding a high-speed CML adder circuit. The adder function is widely used in digital signal processing. The extra adder in the CLB will reduce the number of cells used by such applications.

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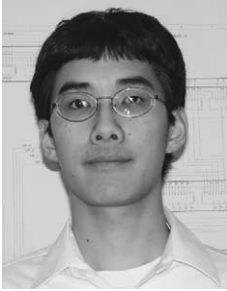
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