

Silicon germanium programmable circuits for gigahertz applications

J.-R. Guo, C. You, M. Chu, P.F. Curran, J. Diao, B. Goda, P. Jin, R.P. Kraft and J.F. McDonald

Abstract: Implementation of a silicon germanium (SiGe) field programmable gate array (FPGA) has been described. The reconfigurable basic cell (BC) that evolved from the Xilinx XC6200 has been redesigned to achieve high speed with lower power consumption. The propagation delay of the BC in comparison to the BC implemented in the earlier generation SiGe process has been reduced to 18% of its original value (from 240 to 42 ps) and the power consumption has been comparably reduced. The range of power reduction is from 13% of its original value when the BC is fully turned on down to 2% when the power saving scheme is applied. A 20×20 SiGe FPGA with physical dimensions of 4.5×4.8 mm has been fabricated using the IBM 120 GHz (7HP) process. To deliver a 10 GHz clock, an H tree has been designed and implemented with reduced skew. To demonstrate its performance, a 4 : 1 multiplexer (MUX) has been mapped for comparison with various CMOS FPGAs. The SiGe FPGA can achieve an 8 Gbps transmission rate, which is a 40 times improvement over the same implementation on a Xilinx Virtex CMOS FPGA. Other comparisons between the SiGe FPGA and commercial FPGAs have also been included. From simulations and measurements, the SiGe FPGAs have been shown to have high performance that can successfully tackle gigahertz applications.

1 Introduction

Field programmable gate arrays (FPGAs), after their introduction by Xilinx, have demonstrated versatility in many fields such as networking and digital signal processing (DSP). However, the relatively low operating frequency of CMOS FPGAs does not meet the requirements of gigahertz applications requiring very high sampling rate data acquisition and processing. In 2000, the first high-speed silicon germanium (SiGe) FPGA and support circuits utilising current mode logic (CML) were proposed [1, 2]. The high performance of CML makes it a good candidate for implementing high-speed FPGAs, however, the large power consumption (108 mW per basic cell (BC) [2]) makes it difficult to scale up the number of BCs. To alleviate this problem, a new SiGe FPGA BC with lower propagation delay and lower power consumption is proposed.

2 Background

2.1 Multi-GHz SiGe processes

Technical progress in developing SiGe heterojunction bipolar transistor (HBT) technology has been exceptionally rapid. The SiGe BiCMOS process has evolved over several

generations, resulting in the HBT's cutoff frequency approaching 120 GHz (7HP), and it is still increasing. Recently, a 210 GHz process (8HP) has been released [3]. Built on a graded Ge alloy base, the Ge content varies linearly across the base to create a built-in electric field that aids the faster movement of minority carriers. This reduces the base transit time to increase its cutoff frequency. SiGe technology offers performance superior to III-V devices with much better yields and lower costs. With this excellent performance, the transmission rate of some SiGe applications has reached 56 Gbps [4]. IBM SiGe 5HP (47 GHz), 7HP (120 GHz) and 8HP (170–210 GHz) processes have been used for the implementation of a SiGe FPGA.

2.2 Current mode logic

CML is a close relative of emitter coupled logic (ECL). Similar to ECL, it is a differential logic design methodology that focuses on steering current from one side to the other in a logic tree with two branches (e.g. from the left to right branch) instead of switching currents on and off. The benefit is much reduced switching noise and fast transitions. The reference current (I_{ref}) is provided at the bottom of the current tree. Using models and transistor parameters to establish the DC characteristics of the CML [5], it has been determined that the input differential voltage should be >120 mV to fully switch the I_{ref} from the left side to the right side, and vice versa. A 250 mV differential voltage is implemented here for added safety margin. See the work of Martin [5] for a full explanation on CML. Therefore the voltage of the input levels is set as Level 1: 0 to -0.25 V and Level 2: -0.95 to -1.2 V with $V_{BE} = 0.7$ V. The power consumption of the CML can be calculated by (1). To reduce the power consumption, a designer needs to decrease the reference current and power supply voltage. The positive and negative power

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J.-R. Guo is with IBM, NY 12533, USA

C. You is with the University of North Dakota, USA

M. Chu, J. Diao, P. Jin, R.P. Kraft and J.F. McDonald are with the Department of Electrical, Computer and Systems Engineering, Rensselaer Polytechnic Institute, Troy, NY 12180, USA

P.F. Curran is with Sierra Monolithics, Redondo Beach, CA 90277, USA

B. Goda is with the Department of Electrical Engineering and Computer Science, United States Military Academy, West Point, NY 10996, USA

E-mail: jrquo2000@gmail.com

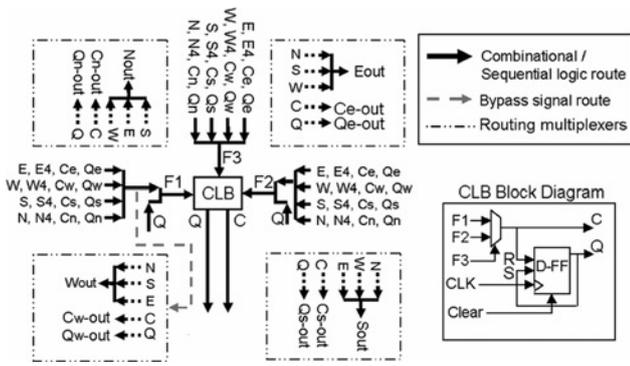


Fig. 1 Schematic of the SiGe BC

Output MUXes of the output routing blocks are shown in dashed blocks

CLB located at the centre is shown in the right-hand side

Others are the input MUXes (F1, F2 and F3) of the input routing block

supply voltages are designated as V_{cc} and V_{ee} , respectively, referring to the conventional connections of the collector and emitter terminals of bipolar transistors in the CML trees

$$\text{Power} = (V_{cc} - V_{ee}) \times I_{ref} \quad (1)$$

3 New Proposed basic cell: emulation of the X6200

Fig. 1 shows the proposed configurable cell that evolved from the Xilinx 6200 [6, 7] and the first SiGe FPGAs [2]. The cell includes input routing block, configurable logic block (CLB) and output routing block. Three input signals coming from its neighbours are routed to the input routing stage. The first group is comprised of the signals from the east, west, south and north (E, W, S and N) neighbours. The second group includes the outputs of the east, west, south and north 4×4 blocks (E4, W4, S4 and N4). The third group consists of the outputs from the D-FF (Q) in the CLB and the combinational and sequential outputs from the nearby cells' logic outputs before the output multiplexers (MUXes) (Cx and Qx). The input signals coming from the neighbours are selected by 17:1 (F1 and F2) and 16:1 (F3) MUXes and their outputs are passed to the CLB. Fig. 2 shows the schematic of the 17:1 MUX in the input routing block, which is composed of 4:1 and 5:1 MUXes. A 16:1 is obtained from the 17:1 by replacing the 5:1 MUX with a fifth 4:1 MUX. Fig. 3 shows the general form of the MUX design. A decoder is added to

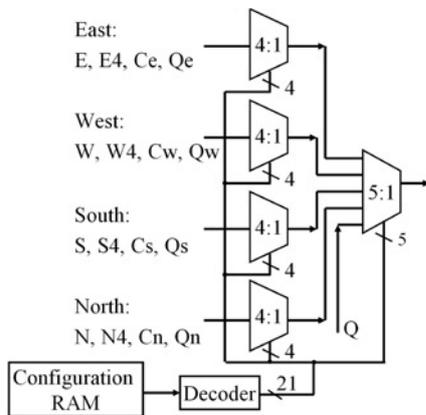


Fig. 2 Redesigned input routing block of the 17:1 and 16:1 MUXes

Label Ce indicates the output of a combinational logic (C) from the east, and so on

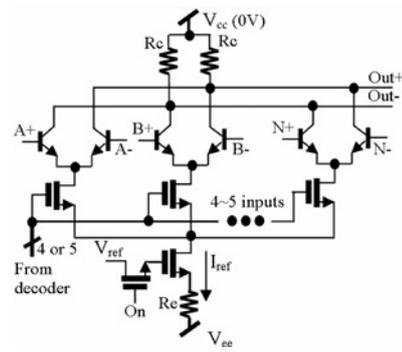


Fig. 3 General form of the new MUX design

New input routing stage has 4:1 and 5:1 MUXes and the new output routing stage has 4:1 MUXes

each MUX to enable the selected inputs and reduce the height of the CML MUX. From (2), the minimum power supply voltage of the new MUX is 2.2 V, where $V_{cc} = 0$ V, $V_{ee} = -2.2$ V, $V_{BE(on)} = 0.75$ V, $V_{DS} = 0.5$ V and $I_{ref} \times R_E = 0.45$ V. Thus, to operate under a reduced supply voltage for overall power savings, the height of the CML tree is limited to two-input levels. A decoder generates an enable signal to turn on one of the N-FET switches for selecting the emitter coupled pair inputs. An N-FET switch is used to turn off the reference current (I_{ref}) of the CML tree if it is not used

$$V_{cc} - V_{ee} = V_{BE(on)} + 2V_{DS(sat)} + I_{ref} \times R_E \quad (2)$$

The D-flip flop (D-FF) used in the CLB has been redesigned to accommodate more functions without increasing the input signal levels. The master latch provides selection between the outputs of the 2:1 MUX and the D-FF. However, the power supply voltage is increased by another V_{BE} voltage drop after inserting another input level. There are techniques [8, 9] to reduce a CML circuit's power supply. These methods focus on how to properly steer the current between independent current trees. The master and slave latches of the new D-FF were redesigned using this design methodology and are shown in Fig. 4. The bottom of the master latch current tree has been divided into two independent trees. Only one of the trees is turned on by enabling either On1 or On2. For example, one can turn on the On1 input (turn off On2) to select the combinational inputs (C) from the 2:1 MUX and turn on On2 (turn On1 off) to select the sequential inputs (Q) of the D-FF. Compared to the propagation delay of a BC, the performance deterioration of the new latches is not that significant. With regard to the output routing block, the combinational outputs (C) and sequential outputs (Q) are directly connected to their neighbouring cells. The output routing block also distributes the feed-through signals of the input routing block to the neighbour cells to provide more routing capabilities allowing fewer routing

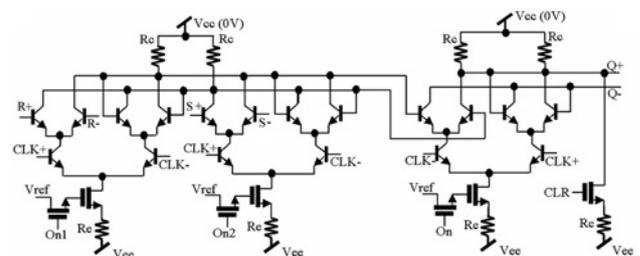


Fig. 4 New D-FF design with 2:1 MUX function built in

Table 1: Power consumption of the different generations of BCs

	V_{cc}, V_{ee}	Process/cut off frequency	Current trees	Reference current, mA	Power consumption, mW	Propagation delay, ps
5HP BC	0, -4.5 V	5HP/40 GHz	30	0.8	108	239
7HP BC	0, -2.8 V	7HP/120 GHz	21	0.7	41.2	100
8HP BC ^a	0, -2.2 V	8HP/210 GHz	21	0.7/0.3 ^b	32.3/13.8 ^b	42/75 ^b

^aSimulation results based on IBM 8HP design kits.

^bHigh performance/power saving modes.

switches to be used. The functionality of the new BC is the same as that of the Xilinx 6200 cell, thus the existing software used to program the Xilinx 6200 cell can also be used to program the new BC. The new BC has dimensions of $170 \mu\text{m} \times 210 \mu\text{m}$.

In the new BC, the total number of current trees has been reduced from 30 in the first SiGe FPGA to 21, and the propagation delay has been reduced by more than half from 239 ps (5HP) to 100 ps (7HP) [2]. From the 8HP simulation results, the propagation delay can be reduced to 42 ps, 18% of the 5HP delay. Table 1 summarises the power consumption and propagation delay values of different BCs implemented in different processes. 8HP simulation results show that if the reference current (I_{ref}) is reduced by half, the BC power consumption is reduced by half, yet the propagation delay (T_p) is still less than that of the 7HP BC. This leads to a noteworthy conclusion: performance can be traded for reduced power consumption.

To further reduce power, a power-saving scheme is also applied to the BC design. The main idea is to turn off the unused blocks in the BC. Several cases are discussed and implemented in the new BC. The possible cases are summarised in Table 2. If the BC is programmed to generate combinational or sequential logic outputs only, the total number of enabled current trees is 7 or 9 (Case A in Table 2). If the signal redirection function is used, MUXes in the output routing block are turned on. Each enabled MUX contributes three additional current trees. These are shown in Case B in the table with different numbers of redirections enabled. If the BC is programmed to perform the redirection function only; the total number of the enabled current trees is listed in Case C. If a BC is not used, the entire cell can be shut down, reducing power

Table 2: Power usage of the multiple power-saving schemes [10]

Design	Tree #	Power usage, %
Case A		
Combinational/sequential logic, no redirection	7/9	33/43
Case B		
Combinational/sequential, one redirection	10/12	48/57
Combinational/Sequential, two redirections	13/15	62/71
Combinational/sequential, three redirections	16/18	76/86
Combinational/sequential, four redirections	19/21	90/100
Case C		
Redirection only per direction	3	14

consumption to a minimum. By applying power-saving schemes (for example: Case A), the maximum power consumption of a BC, compared to the first generation SiGe BC, can be reduced by 90% (10% of the original value) for the 8HP high performance case and by 96% (4% of the original value) for the 8HP power saving mode case.

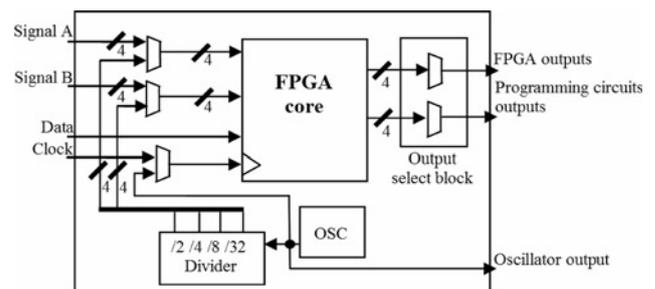
To program the BCs, programming circuitry is designed to serially shift the bit stream by the registers to simplify the whole design [10]. After data shifting cycles, the data are stored in the RAM by asserting Write_EN. The BC is configured by turning on Read_EN. The reason for adding Read_EN circuitry is to prevent random data in the memory from enabling BCs when the chip is powered up. With this design, the programming circuit can store two different configurations and rapidly switch from one to the other.

4 20 × 20 BC array SiGe FPGA

A 20×20 BC array SiGe FPGA composed of the proposed BCs has been designed to achieve its best performance with IBM's SiGe 7HP process. Fig. 5 shows the block diagram of this SiGe FPGA and associated testing circuitry designed to perform 4-bit logic functions. The voltage controlled oscillator (VCO) generates the 10 GHz clock for the frequency divider to get the divide by 2, 4, 8 and 16 periodic signals for testing. An external clock connection is available to provide a second clock source. Two 4-bit MUXes are used to multiplex the external signals and the test signals to the core. The FPGA can be programmed to enable only a partial area to save power. The outputs of the FPGA are multiplexed to the output pads.

4.1 Voltage controlled oscillator

Fig. 6 shows the building block of the feed-forward interpolated voltage controlled oscillator (FFI-VCO), a four-stage ring oscillator designed to run in the frequency range of 7–13 GHz centred at 10 GHz [11, 12]. The capacitor C_c determines the centre of the frequency range. The centre frequency can be calculated by (3) where T_0 is nominal

**Fig. 5** Block diagram of the SiGe FPGA chip

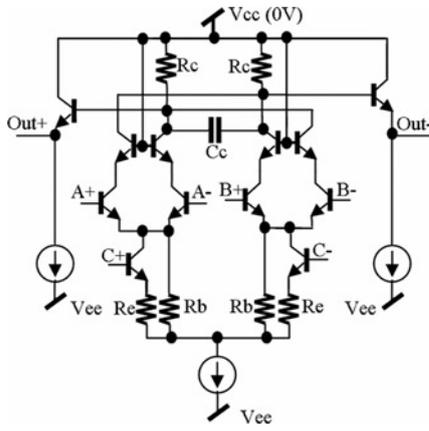


Fig. 6 Building block of the FFI-VCO

delay of the circuit without the capacitor.

$$f_c = \frac{3}{16(T_0 + \ln(2) \times (2R_c C_c))} \quad (3)$$

$$f_{\text{Range}} = \frac{I_0(R_e + R_b) - (v_{be} - (v_d/2))}{8I_0(R_b + 2R_e)(T_0 + 0.7(2R_c C_c))} \quad (4)$$

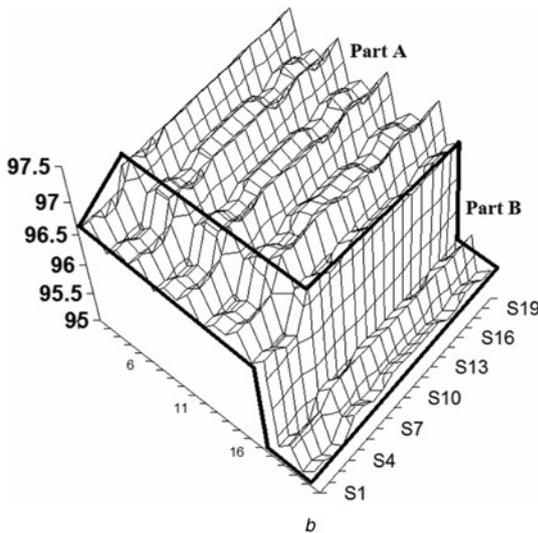
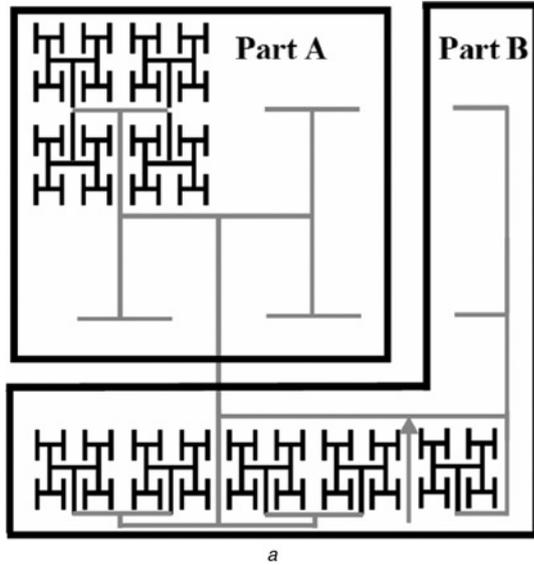


Fig. 7 Clock distribution of the SiGe and stimulated propagation
a Clock distribution
b Simulated propagation delay of clock distribution

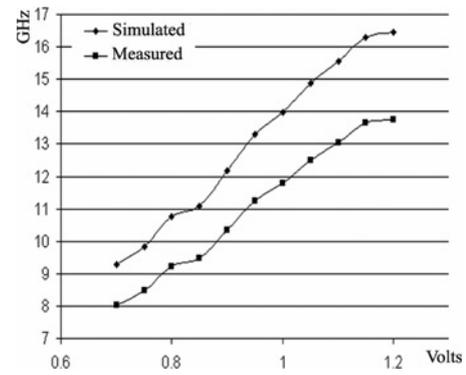


Fig. 8 Simulated and measured VCO operating frequency range (IBM SiGe 7HP process)

Based on the IBM 7HP simulations, T_0 is 21 ps and f_c (centre frequency) is set to 13 GHz. R_c is used to reduce the gain of this circuit to produce a more linear transfer function. The frequency range, which is set to 3.5 GHz, can be determined by (4) where I_0 is the total current through the tree and v_d (i.e. $V_{c+} - V_{c-}$) is the differential input voltage. Each stage receives and linearly interpolates the signals from the previous one and the stage preceding that one. These signals (A+, A-, B+ and B-) are weighted by the control signals C+ and C- and summed by the pull-up resistors (R_c). The minimum operating frequency is defined by the case when the leap signals (B+ and B-) are ignored. In this configuration, the oscillator is running as a four-stage ring oscillator. The maximum frequency can be achieved by selecting the leap signals (A+ and A-) and ignoring the previous stage signals. Thus, the oscillator runs as two 2-stage ring oscillators, which have a higher frequency than the no-leap case. Since the buffer uses a differential circuit, there is no need to add an additional stage to invert the signals to create oscillations.

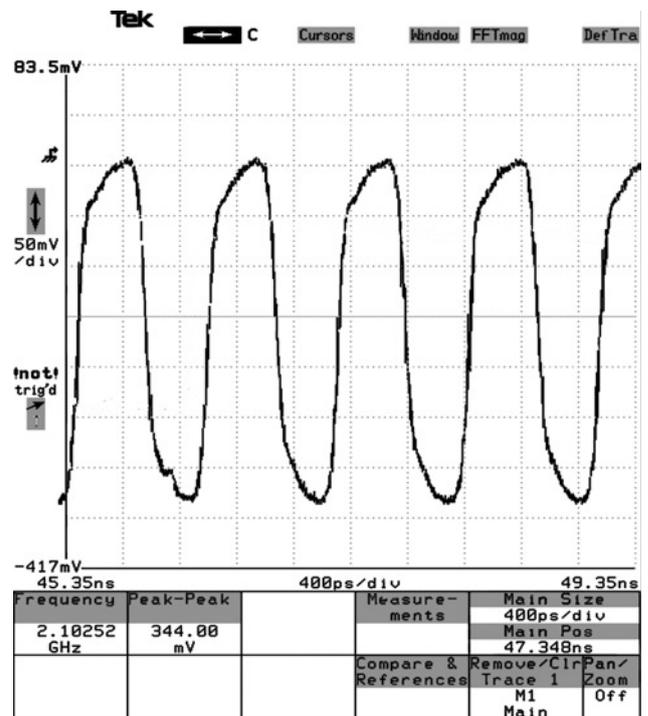


Fig. 9 Measured waveform of the BC ring oscillator (IBM SiGe 7HP process)

4.2 Power distribution and clock tree in the FPGA

A simplified circuit model [13] of on-chip power distribution has been used to calculate the width of the power rail to deliver the voltage with 1% or less voltage loss (a voltage drop from 2.8 to 2.77 V) in the SiGe FPGA. The IBM design manual shows different metal layer parameters used for power rails [14]. The width of the power rail should be 75 μm or more.

A quasi-TEM analysis of on-chip clock wire has been applied to optimise the clock driver placement. Two differential clock signal wires parallel to each other can be treated as two coupled transmission lines in odd mode with a microstrip structure [15]. The equivalent model is shown in the same paper. The conductor and dielectric attenuation constants α_c and α_d are determined first based on previous work considering skin effect and microstrip geometry and reverse calculation.

$$V_{\text{out}} = F^{-1}[\exp(-(\alpha(f) + \beta(f)z)F[V_0])] \quad (5)$$

Equation (5) is used to determine the output waveform at a certain distance in the time domain, where V_0 is the input pulse voltage at $z = 0$, and V_{out} is the output pulse

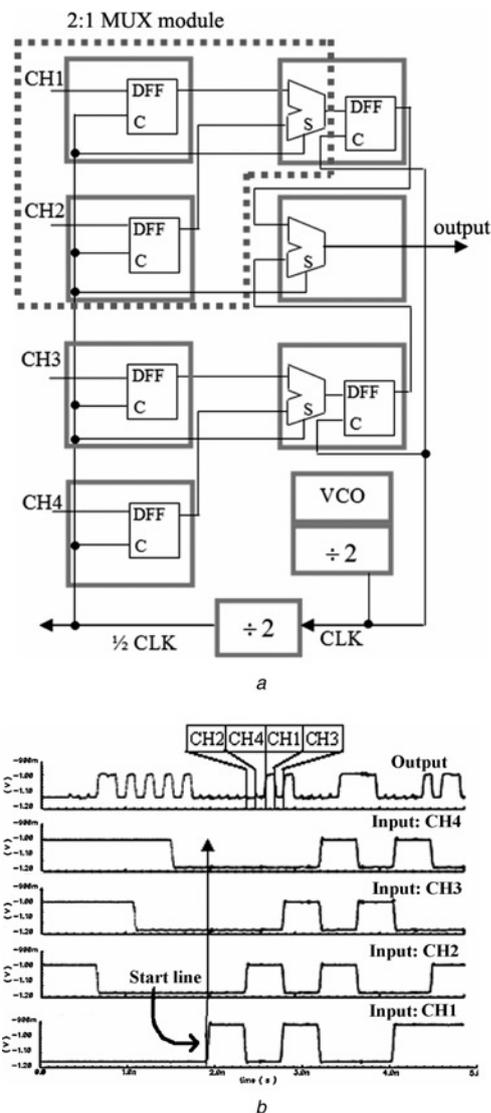


Fig. 10 Routing schematic and simulated behaviour of a 4:1 serialiser

a Schematic of the implemented 4:1 MUX in the FPGA
b Simulated result of the 4:1 serialiser with the 10 Gbps outputs

voltage at distance z along the line, F is the Fourier transform and F^{-1} is the inverse Fourier transform. Based on the model, a clock driver has to be placed every 700 μm if the attenuated clock signal amplitude is to be kept above 90% of its full swing propagating along the wire.

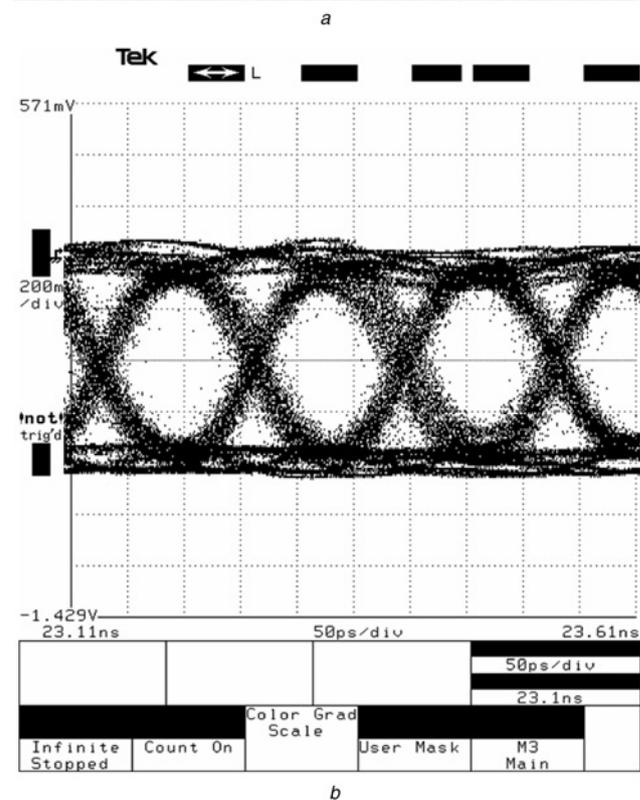
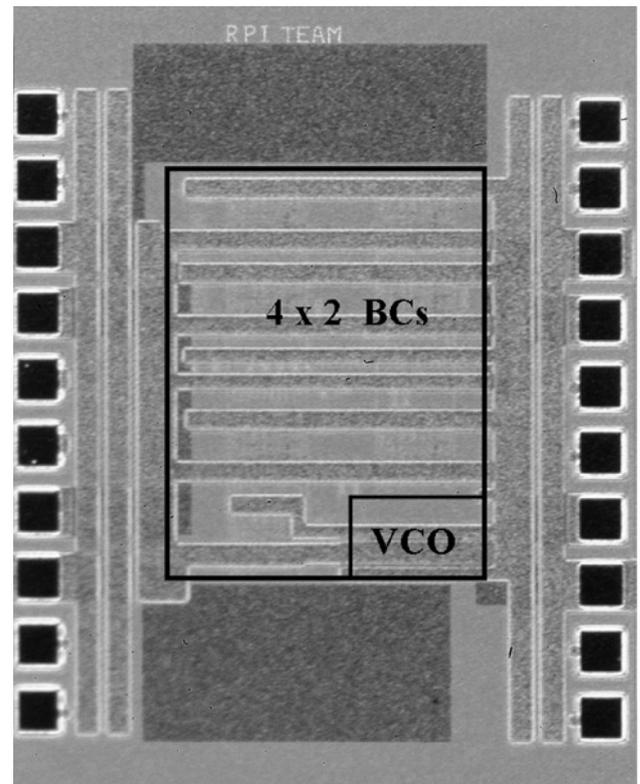


Fig. 11 Photograph of the fabricated 4×2 BC array FPGA and the measured eye-diagram of 4:1 serialiser

a Microphotograph of the fabricated SiGe FPGA chip with 8 basic cells (1.7 mm \times 1.5 mm)
b Measured result from the output pad of the 4:1 serialiser implemented by the SiGe FPGA with a 125 ps period (8 Gbps)

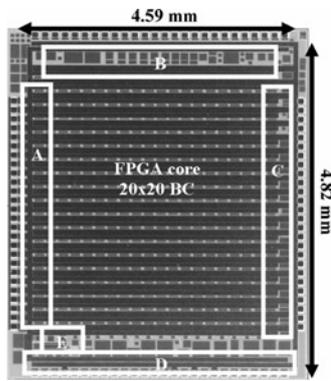


Fig. 12 Micrograph of the SiGe FPGA

otograph of the SiGe FPGA

A: input pads, B: V_{cc} pads, C: output pads, D: V_{ee} pads, E: FFI-VCO

To minimise the clock skew of the clock tree, an H-tree structure is adopted. Fig. 7a shows the clock distribution of the SiGe FPGA. The clock distribution is also performed using differential signalling to avoid introducing phase noise. It is separated into two parts. Part A is the symmetric part (16×16 BC array). Part B is the asymmetric part. Since the new BCs are used throughout the FPGA, the load of each terminal at the end of the clock tree in part A is the same. Since it is an asymmetric layout having identical loading and matching the length of interconnect to reduce the effect caused by parasitic elements is more difficult. Fig. 7b shows the simulated propagation delays of a clock source to all BCs of the design. It can be observed that, in part A, the maximum propagation delay difference of each point is ~ 1 ps. Comparing the propagation delay between parts A and B, the maximum difference is ~ 3 ps, which is more than the largest difference in part A. This result is good for our FPGA, because the variation (3 ps) is small compared to a BC's minimum clock period (100 ps). This analysis only covers layout variation induced skew.

5 Simulation and measurement results of SiGe FPGAs

5.1 Measurement of the VCO

Fig. 8 shows simulated and measured frequency ranges of the VCO. The measured frequency range is between 8 and 13.7 GHz, which is about 86.7% of the simulated results. The measured values are about 17% slower than the simulated values due to parasitic effects.

5.2 Measurements of BCs

Two chips have been fabricated to test the performance of the BC. The BCs in both chips were configured to be ring oscillators. Fig. 9 shows the measurement of the 7HP test chips. From the measurements, the 7HP four-stage ring oscillator has a period of 800 ps. Therefore, the 7HP BC operates up to 10 GHz. From these data, it is shown that the operating frequency has been increased by a factor of two from 5HP to 7HP while achieving a reduction in power consumption of nearly 50% [10].

5.3 Simulations and measurements of a SiGe FPGA application

To further demonstrate the performance of the SiGe FPGA, a smaller implementation of a 4:1 MUX using 8 BCs has been designed and fabricated using the 7HP process. To avoid confusion, the 4:1 MUX is referred to as a serialiser.

Fig. 10a shows the routing schematic of a 4:1 serialiser with the tree architecture, where the building elements are a series of 2:1 serialiser modules shown as the dashed block. It takes four data streams (CH1–4) with a half rate input clock to create the final 4:1 serialiser output. Fig. 10b shows the simulated behaviour of the 4:1 serialiser with a transmission rate of 10 Gbps. Fig. 11a is a photograph of the fabricated 4×2 BC array FPGA and the measured eye-diagram of the 4:1 serialiser, shown in Fig. 11b, indicates it runs at 8 Gbps with an output swing of 700 mV. Compared to the simulation result, the actual performance is degraded by about 20%. Fig. 12 is a photograph of the 20×20 BC array FPGA.

5.4 Performance and power consumption comparison of SiGe and CMOS FPGA

To compare the performance of the SiGe FPGA with CMOS FPGAs, the 4:1 serialiser has been implemented on a Xilinx Virtex™ FPGA using a developer's protoboard. Xilinx Foundation 2.1 software was used to configure the FPGA. Table 3 compares the parameters of circuits mapped and implemented on the SiGe FPGA and Xilinx Virtex FPGA. The latest Xilinx Virtex II Pro FPGA [16] was not available for testing, but it is worth noting that its operating frequency is 710 MHz and register-to-register transfer rate is 1.05 GHz, ~ 3.5 times faster than the earlier version but still one-tenth the speed of the SiGe FPGA. By varying the frequency of the external clock source, the maximum transmission rate that the 4:1 serialiser mapped onto the Xilinx Virtex FPGA could achieve ~ 200 Mbps. When compared to the SiGe result, the SiGe

Table 3: Performance comparison of the SiGe FPGA and CMOS FPGA

Description	SiGe FPGA IBM-7HP		Xilinx Virtex protoboard	
	Operating frequency, GHz	Power consumption, mW	Operating frequency, MHz	Power consumption, mW
4:1 serialiser	8 ^a	146.3	200 ^a	53
4-bit counter	8 ^b	80.84	210 ^a	28
Register-to-register	10 ^a	35.43	283 ^a	12 ^c

Protoboard configuration: Software: Xilinx Foundation 2.1; Chip: Virtex-4 (speed grade). Power consumption calculated from CML configuration and Xilinx worksheets.

^aMeasured values.

^bThe estimated operating frequency of the SiGe FPGA is 8 GHz based on the previous simulation and measurement results.

^cEstimated value based on Xilinx data.

FPGA result is ~ 40 times faster than the Xilinx Virtex FPGA. Based on (1) and BC utilisation listed in Table 2, in the 4:1 serialiser case, the total power consumption is 146.3 mW. To calculate the power consumption of a design mapped onto the Xilinx Virtex FPGA, Xilinx provides a web based work sheet (V1.5) [17]. It is based on the design's resource usage, toggle rates and other factors. By using this work sheet, the power consumption of the same circuit mapped onto the Xilinx Virtex FPGA is 53 mW. From the 4:1 serialiser case, the power consumption of the SiGe FPGA is 2.7 times that of the Xilinx Virtex FPGA.

6 Conclusion

By redesigning the circuitry, adding new options and moving fabrication to the more advanced 8HP SiGe process, the new FPGA BC has a greatly reduced power consumption compared to the first generation while providing increased speed. Previously, cell power consumption severely limited the maximum number of cells that could be integrated in a die therefore with these advancements it is now possible to implement larger arrays with the same power consumption. The new BC has been proven to run up to 10 GHz, clock speeds that are much higher than those of current commercial FPGAs. The high performance of the described SiGe FPGA makes it a good candidate for use in GHz-range data acquisition and other applications requiring high throughput.

7 Acknowledgments

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