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PAPER

High-Speed Reconfigurable Circuits for Multirate Systems in SiGe HBT Technology

This paper describes FPGA fabrics based on high-speed (> 50 GHz) reconfigurable integrated circuits and how they may drive system applications. The authors propose SiGe BiCMOS as an example technology to enable this possibility.

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ABSTRACT | In this paper, we discuss the advantages and opportunities presented by high-speed (> 50 GHz) reconfigurable integrated circuits and how they may drive reconfigurable systems applications, such as software-defined radio, radar, and imaging. We propose silicon–germanium (SiGe) BiCMOS as an example technology that enables ultrafast reconfigurable systems and present several circuit designs based on SiGe heterojunction bipolar transistors (HBTs). We compare circuit designs between generations of IBM's SiGe process, including a recent 9HP process featuring devices with a cutoff frequency (f_T) of 300 GHz. We describe an architecture for an 8-b 80-Gs/s analog-to-digital converter (ADC) and a 48 × 48 cell field-programmable gate array (FPGA), which provide powerful solutions for useful functions, such as digital signal processing (DSP) and polyphase filtering. Other circuit concepts are described, including a voltage-controlled oscillator (VCO) with a tuning range of 26 GHz and a high-performance (80 Gb/s) crossbar switch, which provide utility in reconfigurable system applications. Measured results from fabricated implementations of these described systems are presented. We comment on future prospects of these systems and examine an emerging lateral bipolar device (f_T = 825 GHz) having 100× less power consumption than conventional vertical HBTs.

KEYWORDS | Analog-to-digital converters (ADCs); BiCMOS integrated circuits; field-programmable gate arrays (FPGAs); heterojunction bipolar transistors (HBTs); voltage-controlled oscillators (VCOs)

I. INTRODUCTION

High-speed reconfigurable integrated circuits (ICs) present many advantages for the systems that they construct and enable. Higher operating frequencies and larger bandwidths expand the scope and application of reconfigurable systems while maintaining or expanding upon their typical benefits. Low cost, fast prototyping, and improved efficiency represent only a few of the many benefits reconfigurability traditionally provides for a design solution. With the addition of improved frequency performance, opportunities for new system structures and ICs with high utility are created.

Areas of research that benefit from ultrafast reconfigurability are numerous. In the realm of IC design, software-defined radio is a topic of much interest. A

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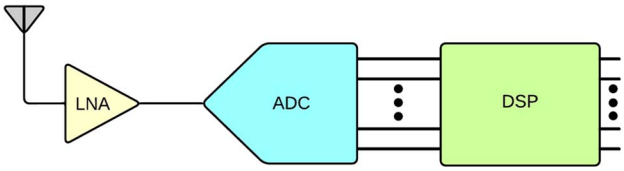

Fig. 1. ***Block diagram of ideal software-defined radio.***

software-defined radio is a programmable device that can be reconfigured using software to operate over large bandwidths [1]. Several strategies for creating adaptable receivers and transmitters have evolved. Using individual broadband elements in a low noise amplifier (LNA), voltage-controlled oscillator (VCO), mixer, or an analog-to-digital converter (ADC) in a singly connected package is one such strategy. An alternate strategy is to employ an array of elements such as those constructed in a field-programmable analog array (FPAA) [2]. Using broadband elements rather than an FPAA can result in significant savings in power and area. Unified receivers and transmitters that are capable of spanning several communication bands are appealing to many in that they allow adaptation on the fly to different standards or between modes of communication [3]. Elevating carrier frequencies with high performing components will facilitate unprecedented data rates that will enable ultrahigh-definition media transfer, improve access to the largest libraries of information, and produce more capable radar [4]. Applications such as automotive radar [5], medical sensors and imaging, and optical communication [6] are among others that would benefit from both the higher frequencies or data rates provided and the ability to adapt that are enabled by these high-speed reconfigurable components.

As the frequency performance of circuits improves, architectures will become closer to the ideal structure and function of a software-defined radio, as presented in Fig. 1. Here, a full Nyquist rate converter with extreme accuracy on the order of 20 b or more would have the capability to ingest the entire radio-frequency (RF) spectrum up to the carrier frequency. Only a quality LNA between the ADC and antennas would be required. In contrast to the strategies previously described where the radio is tuned for a specific application, the whole spectrum received could be segmented and pushed to individual functional blocks or field-programmable gate arrays (FPGAs) to perform digital signal processing (DSP) operations. The ability to process this wide range of the spectrum all at once brings about great utility. The increasing demands of Internet of Things (IoT) devices and the Internet of Everything (IoE) will create a need for larger bandwidth and greater spectrum allocation. Future connected devices will operate at frequencies above 50 GHz and be integrated in such a system. In using more channels in larger spectrum ranges, an ideal software-defined radio could send each channel to a separate functional block to process and effectively increase bandwidth of wireless communication between many devices all at once and on a massive scale. This radio would truly be a multifunctional all-in-one receiver and transmitter.

High-speed FPGAs can provide even more flexibility for a system when used in conjunction with analog or mixed signal elements. FPGAs can be configured into a variety of filters [7], finite impulse response (FIR), polyphase or otherwise, or perform other DSP functions on high rate signals. Apart from the analog domain, FPGAs further epitomize reconfigurability in pure digital operation. Higher performance FPGAs lead to faster prototyping and increased functionality in the growing number of systems where they are being used to replace application-specific integrated circuits (ASICs). Increasing design and production costs as feature sizes have shrunk creates appeal for the use of FPGAs where traditionally only ASICs were employed. High-speed FPGAs can provide low-cost functionality updates and potentially longer lifetimes of deployed systems.

The very fabric of a reconfigurable system can certainly play a significant role in its overall performance. The manner in which signals or data are moved from one element to another is vitally important and can be the bottleneck of design. A high-speed routing element, crossbar switch, or embedded reconfigurable interconnect can be quite desirable within a system, especially in a multirate or interleaved system in which such a device will need to keep up with directing high-speed data that may be from multiple sources. Improving the speed of this routing or switching element can improve bit rates significantly while continuing to provide the ability to adjust cross connectivity. Future routers built in advanced technologies will enable terabit per second performance in software-defined networks. Such performance is increasingly demanded by large commercial data centers.

There are currently several different strategies employed by designers to create systems in the analog and mixed signal domains. Circuits aimed for operation within the 0.1–10-GHz range are typically realized by complementary metal–oxide–semiconductor (CMOS) circuits where their low power, lower area cost, and direct integration with standard cell digital CMOS can be utilized. These implementations are commonly narrowband in nature, which limits their application. CMOS RF kits have been developed to enhance the capability of these devices in the analog and mixed signal space with added features such as thick metal lines. In small lithography CMOS processes, where higher cutoff frequencies are available, design becomes more challenging due to high substrate doping creating lossy substrates. When systems demand high frequencies and large bandwidths, custom silicon–germanium (SiGe) heterojunction bipolar transistor (HBT) circuits are needed at the cost of increased power consumption and area. Bandwidths in excess of 80 GHz with gains of over 20 dB have been reported in SiGe HBT

circuits without requiring the use of inductive peaking or distributed amplifiers [8]. In the mixed signal domain, BiCMOS kits with both HBT and CMOS devices excel by delivering all the performance benefits of the HBT while also providing low-cost and high-density CMOS devices. This allows designing for performance where needed for the most demanding applications while still achieving fully integrated solutions. Strategies such as interleaving can be utilized to bridge the gap between SiGe HBTs and CMOS logic in these systems. There are several candidates a designer may consider as a solution for signal processing. In this setting, CMOS ASICs or DSPs perform well at low frequencies (< 1 GHz) with low power consumption (< 1 W). They are high risk though due to their lengthy time to market coupled with inflexibility. CMOS FPGAs can be configured for this purpose, but cannot alone achieve the speed of the CMOS DSPs due in part to delay from signal routing between cells and long interconnect. FPGAs, however, provide the powerful element of reconfigurability that allows adaptation to the changing demands of a system and alleviates redesign costs. SiGe FPGAs in particular offer much higher functional frequencies (> 20 GHz) and data rates (> 10 Gb/s) than either FPGAs or ASICs realized in CMOS processes. While they are not as dense or as low in power consumption as CMOS FPGAs, SiGe FPGAs become necessary when CMOS realizations cannot deliver the speeds that the highest performing reconfigurable systems demand. SiGe BiCMOS kits have the ability to push reconfigurability across higher operational frequencies and into emerging application spaces.

To meet the demands of high-performance systems, high-speed circuits need to be built using a capable device in an advanced process. SiGe HBTs in BiCMOS technology kits are an appealing solution due to their high cutoff frequency (f_T) and superior noise performance. Operation over vast temperature ranges and radiation hardening make them suitable for extreme environments like those seen in space missions [9] as well. IBM's SiGe process is one of particular ability and interest that will be detailed further in the coming discussion in Section II.

Three-dimensional integration of high-speed reconfigurable circuits presents another opportunity to truly create ultrafast reconfigurable systems. By wafer bonding subsystems fabricated in different technologies, an integrated system that leverages the unique advantages of each of those technologies can be constructed. An example of such a 3-D system is presented in Fig. 2 where a complete programmable wave division multiplexing (WDM) routing system is created by bonding together three wafers. Subsystems in the top tiers are fabricated in SiGe and a high-density bottom tier is fabricated in CMOS. The top tier consists of several optical transceivers and a large crossbar switch. The crossbar routes signals to high-speed ADCs on the next tier. SiGe FPGAs would then process data from the ADCs and then pass information to CMOS FPGAs at the lowest tier. Here, low-cost, high-density CMOS FPGAs would perform less performance critical tasks and those highly parallelizable. Current commercial CMOS FPGAs utilize DSPs operating between 600 and 700 MHz. The SiGe FPGAs, however, would need to match the speed of the ADC and consequently operate at a much higher speed than the CMOS FPGAs. Future SiGe FPGAs would be capable of DSP cells operating at 20 GHz or more. At the top tier of the system only a small number of input/output (I/O), on the order of 10–20, are required due to the multitude of information transferred in each wavelength multiplexed stream and the data rates enabled by the SiGe circuits. Challenges to such a system would be the increased production costs involved in wafer bonding and the thermal management of the wafer stack. The wafers to be bonded need to be evaluated to make sure they are known good parts prior to integration to improve yield.

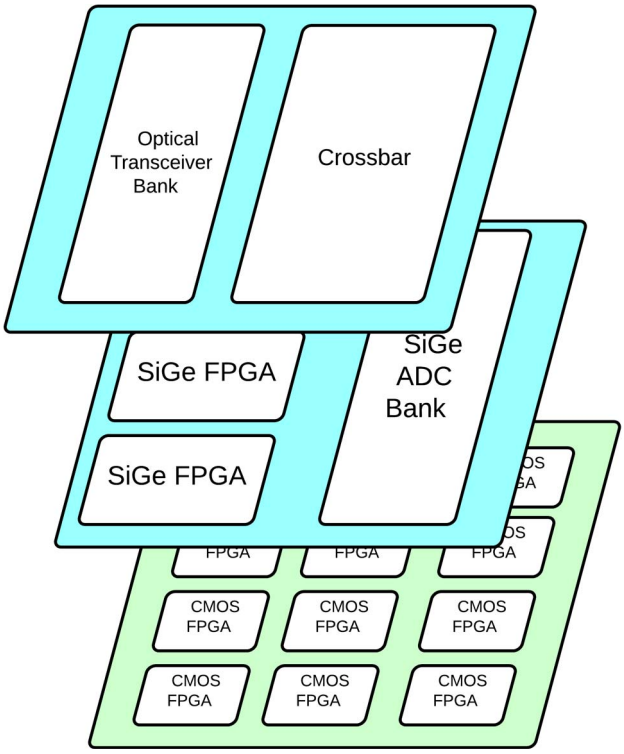

Fig. 2. ***Diagram of wafer bonded 3-D reconfigurable system.***

In this paper, we look to explore high-speed reconfigurable circuits built utilizing SiGe HBT technology. In Section II, we further discuss SiGe technology itself and a circuit topology that suits high-speed design well. Section III presents several different SiGe circuits for reconfigurability in an ADC, FPGA, VCO, and crossbar switch that are well suited for a variety of applications. Measured results from fabricated systems are presented. The future of high-speed reconfigurable circuits and a discussion on a newly emerged lateral bipolar device that may enable them are discussed in Section V. We then conclude with closing remarks in Section VI.

II. TECHNOLOGY AND CIRCUIT TECHNIQUES FOR ULTRAFAST RECONFIGURABILITY

IBM's SiGe BiCMOS technology has emerged as a commercially viable option for the design of high-speed reconfigurable circuits and systems. In this section, first we examine the SiGe HBT device itself and then discuss a circuit topology using SiGe HBTs for use in mixed or digital systems.

A. Benefits of SiGe

Several bandgap engineered materials have emerged as solutions for high-speed transistors, including GaAs, InP, and SiGe. However, only SiGe devices achieve a high-performance level with full integration with silicon CMOS while allowing for high function density as well as large wafer sizes [11].

Silicon germanium devices are created by selectively introducing 3%–9% mole fraction of germanium into the base region of the bipolar transistor [12]. The presence of germanium in the base forms a graded heterojunction, creating a drift field as shown in Fig. 3. This field accelerates the movement of minority carriers, reducing base transit time. The heterojunction enhances electron injection, producing a much greater current gain for the same doping level when compared to silicon transistors [10]. This greater current gain can be traded for improvements in frequency response and noise factors, making SiGe HBTs especially valuable for mixed signal applications.

Recent developments of the IBM SiGe transistor have continued to yield significant improvements over previous generations. Table 1 illustrates the f_T and feature size of the most recent releases of IBM's SiGe kits. By using vertical profile scaling, reduced lateral dimensions, and an improved process integration scheme, the 8HP transistors have been shown to be 70% faster than the previous generation 7HP [13]. 9HP has even further improved upon 8HP moving from a 210-GHz f_T device to a 300-GHz f_T device. Parasitic effects have been shown to affect SiGe devices more than III–V semiconductors, primarily because of their use of semi-insulating substrates. Thus, the reduction in parasitic effects by scaling dimensionally in SiGe results in a much greater performance gain [14].

Table 1 IBM SiGe Process Generations

IBM SiGe BiCMOS Kit	HBT f_T	CMOS Feature Size
7HP	120 GHz	180 nm
8HP	210 GHz	130 nm
9HP	300 GHz	90 nm

B. Current Mode Logic

Current mode logic (CML) is a differential logic family that offers several advantages over single ended logic and emitter coupled logic (ECL). Using a constant current approach, current is routed through branches of a fully differential tree structure, minimizing the need to switch circuits on and off. This static power dissipation results in higher power consumption than traditional CMOS logic, however it drastically reduces the inductance effects and power supply switching noise from on/off switching of devices. This reduction in substrate and power supply switching noise allows digital CML logic to be used with analog components with minimal noise introduced through the power rails.

To maximize performance, CML designs operate with small voltage swings near logic-low (V_{IL}) and logic-high (V_{IH}) of the device. Small voltage swings of 250 mV allow for fast nonsaturated switching and therefore higher

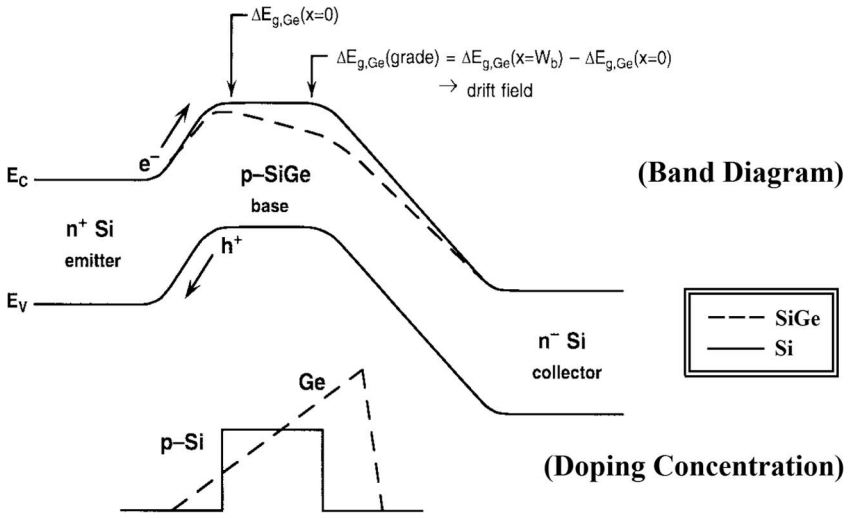

Fig. 3. *Energy band diagram of a graded base SiGe HBT compared to Si BJT [10].*

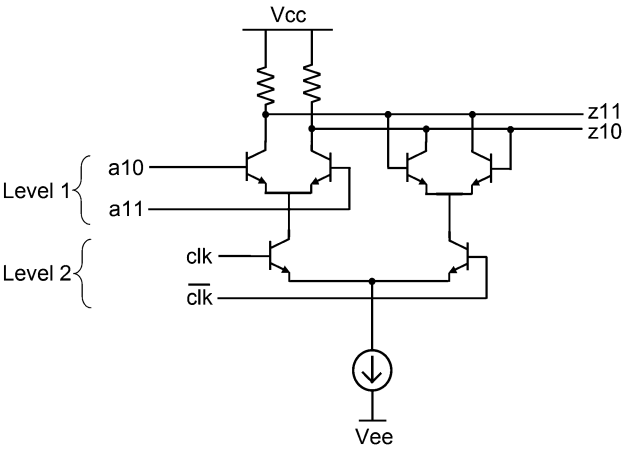

Fig. 4. *Schematic of a CML latch.*

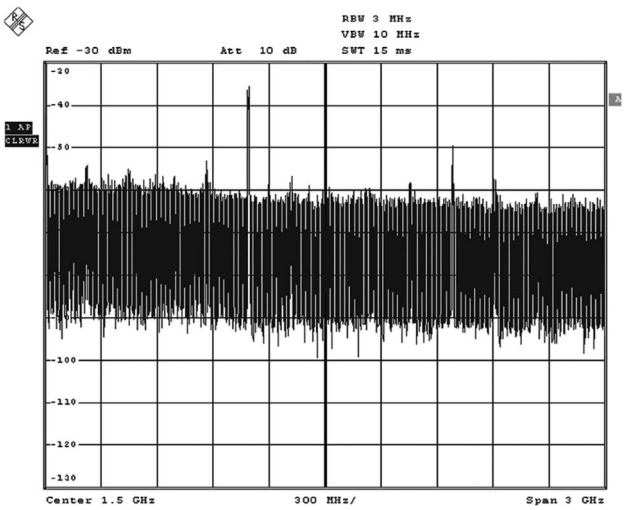

Fig. 5. *Measured output spectrum of 4-b 40-Gs/s ADC [15].*

operating frequencies than conventional CMOS logic. The smaller voltage swings also permit the use of multilevel logic at intervals of the threshold voltage with a low-voltage power supply. The number of voltage levels that can be used is dependant upon the power supply voltage; two voltage levels can be used with a −2.5-V power supply—(0 V to −250 mV, as level 1) and (−900 mV to −1.15 V, as level 2). A −3.4-V supply, however, can provide sufficient voltage headroom for an additional threshold drop and hence a third level of logic in the CML tree structure. Fig. 4 shows an example of a standard CML latch. The small voltage swings and lower level dependence on the upper power supply voltage increase the need for a stable power supply. Noise in the upper supply voltage will more readily propagate into the circuit. As a consequence, a negative power supply is utilized so that the stable earth ground (0 V) can be used as the upper voltage.

III. ARCHITECTURES OF HIGH-SPEED CIRCUITS FOR ULTRAFAST RECONFIGURABLE SYSTEMS

In this section, we discuss circuits and systems that demonstrate the ability of SiGe HBTs to bring high performance to reconfigurability. Some of the circuits developed have been implemented in multiple of IBM's SiGe generations and comparisons between them are made where appropriate.

A. High-Speed Analog-to-Digital Conversion

Analog-to-digital conversion has been a very active research topic in recent years. A high-speed ADC is vital to massively broadband communication systems and will ultimately impact the data rates they achieve [4]. To address these and other performance concerns the authors have looked to build upon successful development of a 40 gigasamples per second (Gs/s) 4-b ADC [15]. This four channel interleaved flash architecture achieved a 3.5 effective number of bits (ENOB). A measured output spectrum is presented in Fig. 5. The complete ADC occupies 1.5 mm^2 and draws 2.1 A with support circuitry from a −3.4-V supply. Each individual ADC channel consumes 1.36 W while operating at 10 Gs/s.

To further push the envelope of converters, the SiGe ADC design has been expanded to eight channels and 8 b in a 9HP implementation. This eight-way interleaved ADC consists of eight individual converter units operating in parallel at 10 Gs/s with a multiphase clock source. With a combined sample rate of 80 Gs/s, this type of converter is useful for digitizing oscilloscopes, radar applications, satellite communications, and optical dispersion correction when coupled with polyphase filtering.

1) Individual ADC Channel Overview: A wide variety of analog-to-digital (A/D) architectures have been developed over the years, however only a few are applicable for high-speed applications. Purely flash converters have been developed using SiGe BiCMOS [17], [18], however their bit accuracies are limited by the number of comparators needed and the enormous input capacitance generated by placing numerous transistors in parallel. The two-stage A/D converter architecture [19] is chosen for this design due to its positive tradeoffs between speed, power, and complexity. A block diagram of a two-stage converter is shown in Fig. 6.

In this structure, analog-to-digital conversion is performed in two steps. The analog signal is first sampled and held by a sample-and-hold amplifier. The output is then passed to a coarse A/D subconverter. The output of the coarse A/D is reconverted to an analog signal and subtracted from the value of the sample-and-hold amplifier to generate a voltage representing the error of the coarse A/D. This residue signal is then amplified and passed to a second

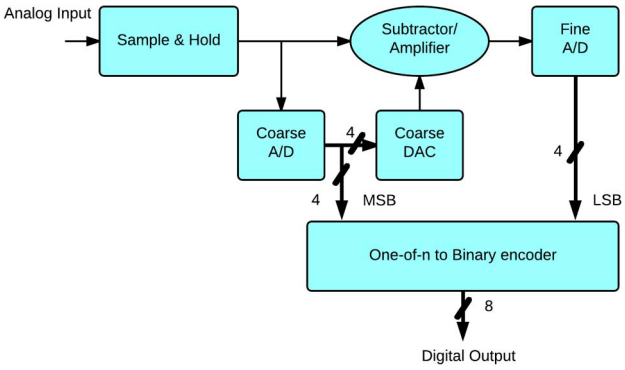

Fig. 6. ***Block diagram of single two-stage ADC channel.***

A/D subconverter stage, whose output represents the LSB of the total two-stage converter binary output. The sample-and-hold amplifier must operate at half the frequency of the rest of the converter for its held output voltage to remain steady long enough so that the output of the coarse stage can be subtracted from it.

To achieve the highest performance within the two-stage A/D converter structure, flash converters are used for both the coarse and fine subconverters. This method drastically reduces the number of comparators needed for the conversion. The minimum number of comparators needed for a standard flash converter increases exponentially, following

$$N_c = 2^n - 1 \tag{1}$$

whereas the minimum number of comparators needed for the two stage flash converter is determined by

$$N_c = 2\left(2^{\frac{n}{2}} - 1\right). \tag{2}$$

N_c is the number of comparators required and n represents the resolution of the ADC.

From these equations, it can be seen that a standard 8-b flash converter requires a minimum of 255 comparators whereas a two-stage flash converter only requires 30 comparators. As noted above, this reduction in complexity comes at the expense of halving the maximum operating frequency. For an HBT-based ADC, the reduction in comparator count is especially important since it reduces the total input capacitance of each flash stage substantially as well as the overall dimensions of the converter.

2) Thermometer Code Error Correction: Flash converters are inherently susceptible to metastability errors caused when the input value is near the reference voltage of a given comparator at the time the output is latched. When the input and reference voltage are near each other, the settling time for a determinate comparator output takes longer to appear, thus the problem gets worse as comparator frequencies increase. To prevent these thermometer code bubbles, the output of a given comparator and the two preceding it are compared, as presented in [20] and [21]. This technique allows the suppression of single comparator errors, and converts the thermometer code to the 1-by-n format before passing it to the encoder circuitry.

3) Time Interleaving: Implementing separate channels to perform staggered A/D conversions offers a way to utilize the increased accuracy that slower A/D conversion provides while maintaining high-speed output. Analog-to-digital converter works by Shiller and Byrne [22] and Poulton *et al.* [23] describe similar systems. In [22], with four-way interleaving, a 4 Gs/s 8-b flash converter was realized in a Si BiCMOS process with a f_T of 12 GHz. In our design, we revisit this approach using IBM's 9HP BiCMOS libraries in which the bipolar devices have a maximum f_T of approximately 300 GHz. With a SiGe sample-and-hold amplifier, the higher clock frequency requires fewer parallel channels, resulting in lower accuracy degradation due to phase mismatches and jitter between channels. Sample-and-hold performance for high-speed analog signals is improved as well. In this architecture, the ability of the front–end sample-and-hold architecture will largely determine overall performance. It is the sample-and-hold amplifier that matches the analog waveform during the sampling period and then holds it steady to present to the individual channels. Each channel has a sample-and-hold amplifier that runs at a fraction of the speed of the front–end relative to the number of channels, in this case eight times slower. Using a front–end sample-and-hold amplifier is advantageous in that it assists in eliminating timing mismatches between channels that would degrade the ENOB. An improved switched emitter follower topology sample-and-hold amplifier with feedforward capacitors is utilized to reduce voltage ripple at the output and improve settling time.

Fig. 7 presents the complete eight-channel ADC layout and a closeup view of one individual ADC channel. The blocks labeled "digital encoder" contain the thermometer code bubble suppression and error-correction circuitry, as well as the 1-by-n to binary encoder.

B. High-Speed FPGA

A high-performance FPGA is useful in a variety of settings. Many designers make use of FPGAs for their ability to prototype and evaluate designs quickly. As their frequency performance has improved, they have become more of a viable option for other applications. Digital communications in particular has become one such area presenting opportunity for SiGe FPGAs. Traditionally, designers have chosen either ASICs or DSP processors for implementation of components like finite impulse response (FIR) filters or

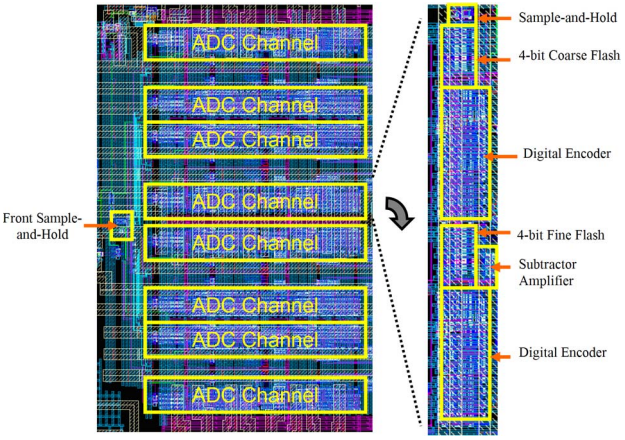

Fig. 7. *Layout of 8-b 80-Gs/s ADC in 9HP.*

infinite impulse response (IIR) filters that are used to improve the accuracy and reliability of communications. ASICs are often employed where performance of these functions is critical and available DSP processors are unable to meet the specifications required. ASICs, however, can be costly to design and manufacture when produced in low volume. FPGAs present themselves well as another alternative. Due to their large capacity, single FPGAs can implement several different operations and configure them on the fly saving cost on future redesign and fabrication. An FPGA's capacity also allows for large scale parallelization of computation and as a result can potentially achieve the same performance as an ASIC.

DSP functions commonly require the use of a multiply accumulator (MAC) unit in which several products are required to be summed together. The addition function often requires numerous cycles to complete and typical DSP processors only contain one MAC unit. FPGA implementations can be expensive in area and resources, especially in realizing a multiplier where a significant number of full adders are required. A typical realization of a 4-b multiplier requires 12 full adders and has a critical path through six full adders. In order to efficiently use a SiGe FPGA as a solution in a DSP setting this challenge had to be addressed. An example of which is an implementation of a FIR filter in SiGe in which lookup tables (LUTs) are utilized. Fig. 8 shows the implementation of this 4-b four-tab parallel FIR filter. The multiply operation is performed in this structure in LUTs in which the results of the operation are preprogrammed. A pipeline stage after each LUT and adder reduces the critical path to that of a 5-b adder. We have found in measurements that a 5-b pipelined adder implemented in our FPGA can run at speeds up to 10 GHz.

Several generations of SiGe FPGAs have been developed using different IBM technology libraries. The latest revision, a 48 × 48 SiGe FPGA, has been designed with the IBM 8HP BiCMOS process and is configured to receive and process outputs generated from an ADC front–end. In the coming discussion, the basic FGPA structure is detailed and performance comparisons are made across IBM SiGe generations.

1) FPGA Basic Cell: Fig. 9 shows the block diagram of the FPGA core, the basic cell (BC). This basic structure is proposed in [26] and has three parts: an input routing block (IRB), an output routing block (ORB), and a configurable logic block (CLB). In the figure, "N," "E," "S," and "W" in signal names designate direction in or out of the basic cell to or from the cell's nearest neighbors. Those

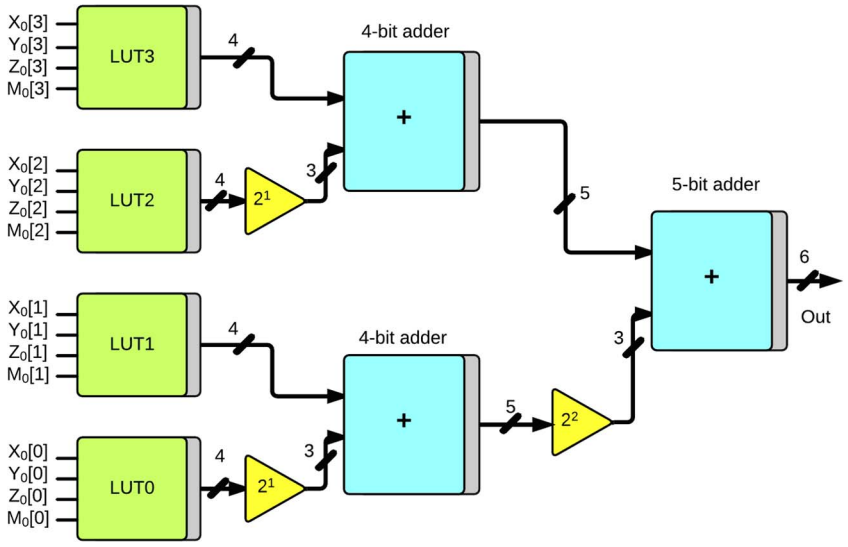

Fig. 8. *Four-bit four-tap parallel FIR filter implemented in the SiGe FPGA.*

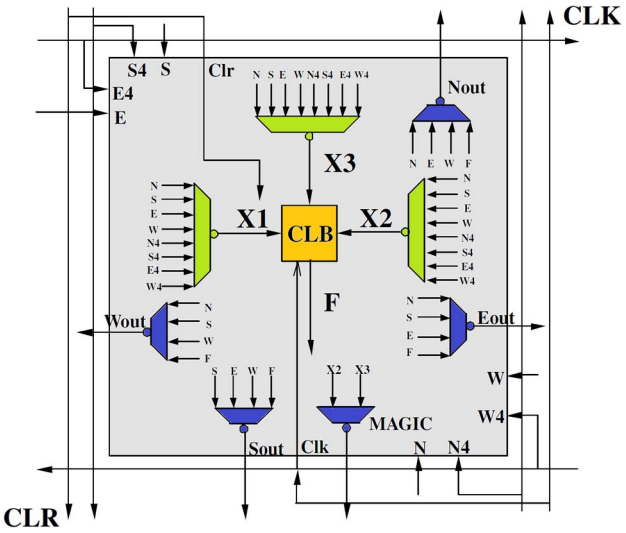

Fig. 9. *Diagram of basic cell core in FPGA.*

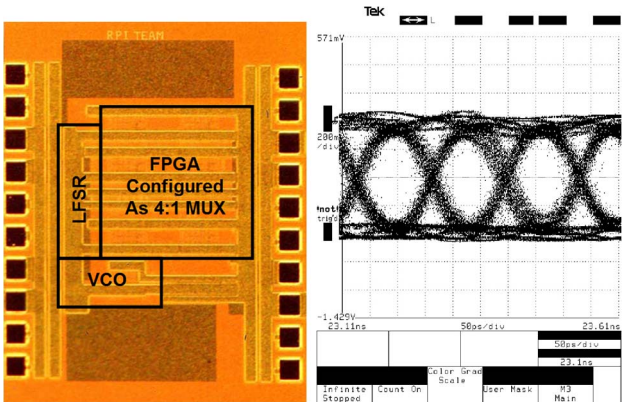

Fig. 10. *Micrograph of FPGA implemented as a 4 : 1 multiplexer (left) and measured eye diagram at 8 Gb/s (right).*

with names ending in a "4" correspond to those to or from a cell four cells away in that direction. The incoming signals are routed to the IRB seen in green which has three 8 : 1 multiplexers that generate "X1," "X2," and "X3." These outputs are then routed to the CLB to perform the desired logic function, the result of which is then passed to the ORB. The ORB is made up of several multiplexors seen in blue that pass the outputs of the basic cell (F, Eout, Wout, Sout, and Nout) to the corresponding neighboring cells.

At the circuit level of the basic cell, focus has been made in modifying CML structures for reduced power consumption. In each CML tree, an NMOS transistor has been added between the voltage reference and each HBT current source it controls. This allows unused trees to be turned off dynamically when not in use for a given programmed configuration. A new combined function CML-based multiplexor merged with a D flip-flop has assisted in reducing the number of CML trees required. These strategies have resulted in the basic cell having a reduced range of 7–21 CML trees on at a given time depending on the programmed function.

A 10-GHz FPGA configured as a 4 : 1 multiplexer has been fabricated to measure the performance of the FPGA basic cells. It accepts four separate data streams and combines them into a single data stream at four times the speed of the original signals. The 4 : 1 MUX has been shown to be capable of generating a 10-Gb/s multiplexed output data stream in 7HP. The inputs of all four data streams are generated by a pseudorandom binary sequence (PRBS) from a linear feedback shift register (LSFR) with a clock source generated by an on-chip VCO. A micrograph of a 4 : 1 MUX test chip and an output eye diagram are shown in Fig. 10. The implementation consumes 146.3 mW from a −3.1-V supply. In our experiments, a similar Xilinx Virtex-E FPGA produced in a 0.18-μm CMOS process consumes 60% less power, but maximally operates at 183 Mb/s when configured as a 4 : 1 MUX.

2) SiGe Technology Comparison: The basic cell is the core component of the SiGe FPGAs. For this reason, it can be used as the basis for performance comparisons across SiGe generations.

The layouts of the 7HP and 8HP generations are 170 × 210 μm^2 and 130 × 138 μm^2, respectively. As shown in Fig. 11, the cell size in 8HP has been significantly reduced through HBT deep trench (DT) sharing techniques [24] and smaller CMOS dimensions of the 8HP SiGe technology. The DT placement around a transistor is a technique that increases transistor isolation, which is beneficial for mixed mode circuits. At the same time, it also has the effect of increasing the minimum spacing between transistors, which is detrimental to digital circuit design because it decreases the total transistor density and increases overall layout size. Techniques have been used to share the deep trench between sides of neighboring transistors,

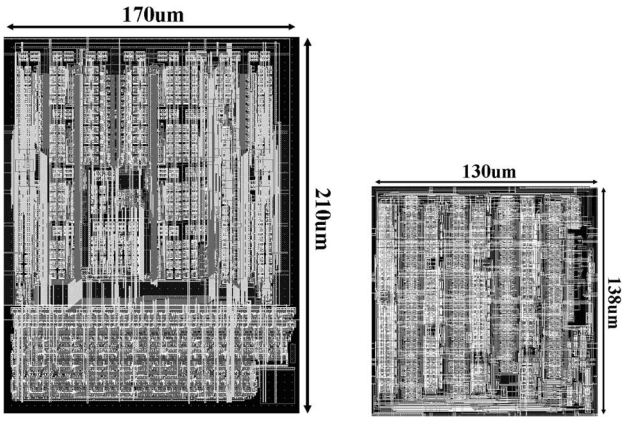

Fig. 11. *7HP basic cell dimensions of 170 × 210 μm^2 (left) and 8HP basic cell dimensions of 130 × 138 μm^2 (right) [25].*

Table 2 FPGA Basic Cell Comparison Across SiGe Generations

Basic Cell Process Generation	Power Consumption per CML tree	Power Consumption (P_{on})	Propagation Delay (T_p)
7HP [24]	2.24 mW	47.04 mW	100 ps
8HP[1] *(high performance case)*	1.54 mW	32.34 mW	42 ps
8HP[1] *(power saving case)*	0.66 mW	13.86 mW	75 ps

1. In high performance case transistors are biased to the maximum cutoff frequency in 8HP. In power saving case transistors are biased at the current corresponding to the peak cutoff frequency as it was in 7HP

therefore saving a significant amount of space when multiple sides are shared.

To make the FPGA as energy efficient as possible, a power saving scheme, as discussed previously, has been developed to turn off the unused current trees. The number of current trees needed varies with the different modes of operation that a basic cell can be programmed into. Table 2 lists the power usage and propagation delay of the basic cell in 7HP and 8HP implementations. Two entries are made for 8HP to reflect the tradeoff a designer can make between current and performance. It illustrates that moving to a more advanced node will lower power consumption and improve performance. It is a design choice as to what degree of each is achieved. In the 8HP high-performance case, for example, a 60% improvement is seen in the propagation delay while still achieving 31% reduction in power per CML tree.

C. ADC With FPGA for Polyphase Filtering System

An ultrahigh-speed ADC with a powerful FPGA allows for many possibilities, especially in DSP. The FPGA can apply digital filtering internally, or it can be used to further deinterleave the signal to slower speeds where low-cost, high-density CMOS can be used to apply complex procedures, and then interleave the filtered data back to a high-speed data stream. Use of an FPGA in place of traditional ASICs for filtering also allows the use of interchangeable multiple filtering personalities and easy application of updates to the filtering algorithm.

SiGe BiCMOS is unrivaled for this type of mixed mode design, since it allows the superior gain, switching speed, and driving capability of bipolar transistors to be mixed with low-cost, high-area-density CMOS logic so that the best of both transistor types can be harnessed.

The top level architecture of the interleaved SiGe filtering system is shown in Fig. 12 while a layout is presented in Fig. 13. Eight separate two-stage converters are parallelized by means of an eight phase clock. The individual 10-GHz ADC channel outputs are passed directly to a 10-GHz FPGA for digital filtering, signal processing, or demultiplexing.

Polyphase filtering is an ideal application for an interleaved ADC–FPGA system. By using time interleaving, the difficult task of filtering a high-speed signal can be split from a single filter to multiple filters running at slower speeds. Fig. 14 shows a block diagram of such a system

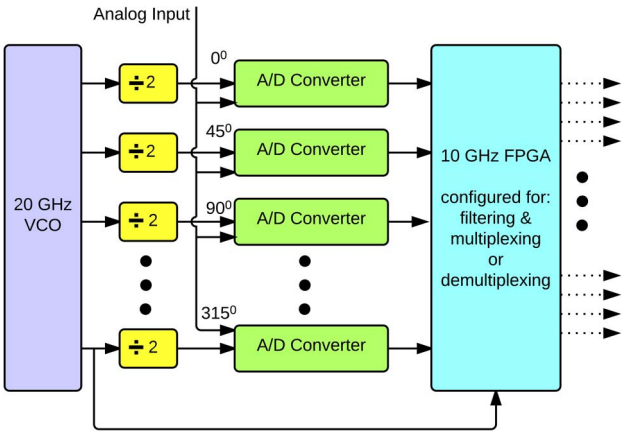

Fig. 12. *Block diagram of the SiGe filtering system.*

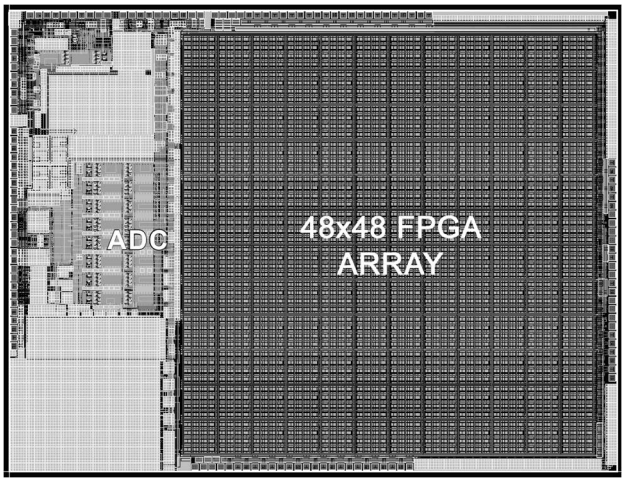

Fig. 13. *High-speed reconfigurable filtering system.*

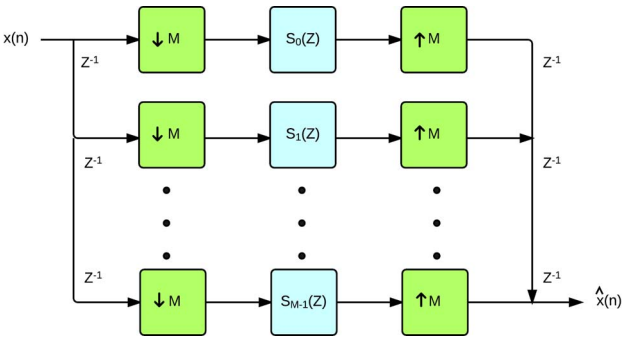

Fig. 14. *Diagram of a polyphase filtering system.*

where a high-speed signal $x(n)$ is decimated into "n" channels before the filter $s_n(z)$ is applied. The filtered signals output are then merged back into a high-speed stream [27]–[29]. Dividing a signal into "n" channels each running at $1/n$ speed allows for low-cost, large-capacity CMOS FPGAs to be used to perform the filtering function, whereas traditionally, expensive ASICS would need to be developed. The reconfigurable nature of FPGAs presents another advantage over traditional methods in that they can be reprogrammed to implement a different filtering function, or even to switch between two functions.

As the data rate envelope of optic communication continuously increases, high-performance and high-speed optical signal equalization is becoming even more critical. Conventionally, equalization is done in the analog domain largely because of the insufficient speed of digital circuits. Although they are able to achieve very high-speed, analog equalizers suffer from significant performance degradation not seen in digital equalizers. The presented SiGe circuit architecture can be combined with multirate adaptive filtering to design an adaptive equalization system in the digital domain for high-performance optic communication.

A multirate adaptive filtering structure has fourfold advantages.

1) The required multiplication operations per sample time simply decreases as decimation factor increases, which is highly desirable for high-speed systems like optic communication.
2) In contrast to other high-speed adaptive filtering methods, such as using a block-processing-based structure, multirate adaptive filtering only performs in the real domain without incurring any FFT/IFFT.
3) A multirate filtering structure is highly parallelizable in nature, which is inherently favorable for high-speed, low-power implementation.
4) The multirate feature can also help to improve the convergence performance of adaptive filtering. In this context, the widely used least mean square (LMS)-based adaptation algorithm is favorable because of its reasonably low implementation complexity.

Equalization for high-speed optic communication is a perfect application when combined with multirate LMS adaptive filtering and the SiGe architecture presented above. In addition to optic communication, such a multirate LMS adaptive equalization system can be used for many other real-life applications such as gigabit per second satellite communication and high-speed wireless local area network.

D. VCO Design

A VCO is an important component of any transmitter or receiver because its tuning range provides the ability to adapt and reconfigure to different signal frequencies and communication standards on the fly. Multiband multistandard receivers are made possible by having the ability to select the frequency of their oscillation. This ability is desirable in radar applications and millimeter wave tuners. In a digital BiCMOS setting, reducing clock speed can provide a means for power saving as it lowers dynamic power consumption.

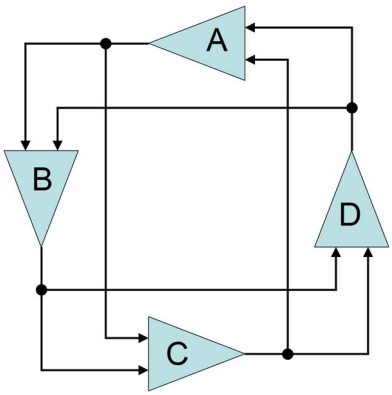

Fig. 15. ***Block diagram of FFI–VCO [30].***

A unique wide bandwidth VCO design has been in development at the Rensselaer Polytechnic Institute (Troy, NY, USA) [30], [32], [33]. Originally fabricated using the GaAs HBT process in [31], the design has been adapted for use with the SiGe libraries from 7HP through 9HP. Fig. 15 shows the block diagram of the feedforward interpolated voltage-controlled oscillator (FFI–VCO) design.

The VCO is formed using four identical stages linked in series where each stage is capable of linearly interpolating the input signals received from the stage preceding it and two stages preceding it. With this configuration, the gate delay of a stage can be tuned to a value between the two signal inputs. For example, from Fig. 15, the output signals of buffer B depend on the signals from buffers A and D. Fig. 16 shows the schematic of the buffer used in the VCO. Its differential input signals "V_i" and "V_j" are weighted by

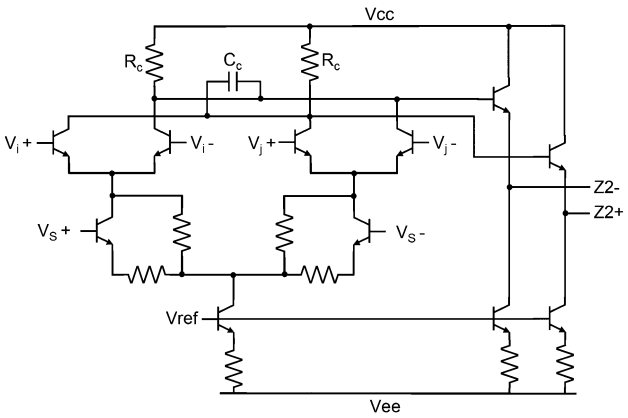

Fig. 16. ***Schematic of FFI–VCO.***

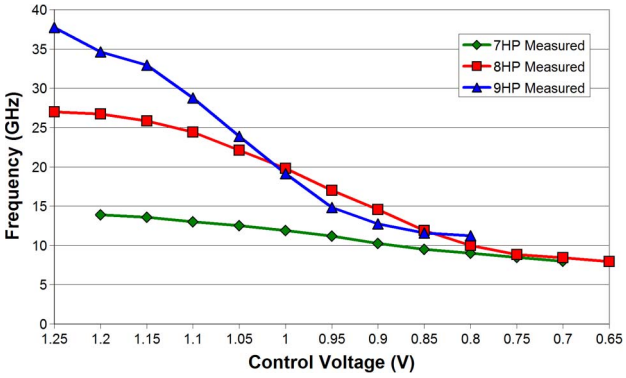

Fig. 17. ***Measured frequency range of the FFI–VCO in different SiGe generations.***

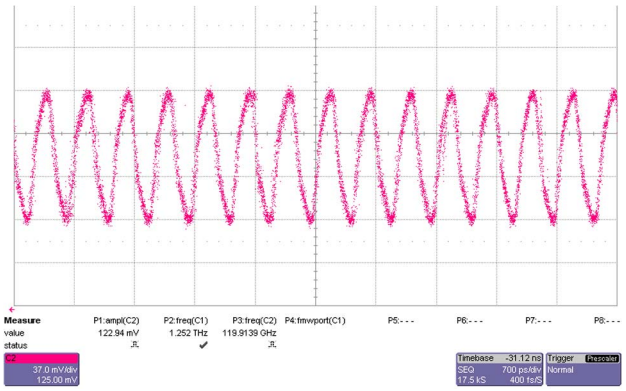

Fig. 18. ***Measured 9HP waveform of FFI–VCO. VCO output of 35.9 GHz divided by 16 to 2.242 GHz seen at scope ($V_{in} = 1.25$ V).***

the differential control signal "V_s" of the buffer and summed by the pull-up resistors (R_c).

The minimum oscillation frequency is obtained when the leap signal, the input from two stages before, is ignored and the VCO is running as a four-stage ring oscillator (A–B–C–D). The maximum frequency can be achieved by ignoring the preceding stage signal, thus causing the VCO to run as two separate two-stage ring oscillators (stages A–C and B–D). Note that with differential signals it is not necessary to use an odd number of stages in a ring oscillator, since a signal can be inverted simply by swapping the outputs of a stage. The center frequency can be calculated using

$$f_c = \frac{3}{16(T_0 + \ln(2) \times (2R_cC_c))} \tag{3}$$

where T_0 is nominal delay of the circuit without the capacitor.

Fig. 17 shows the measured VCO frequency range versus the input voltage of 7HP, 8HP, and 9HP implementations. This four-stage VCO has been measured to have a range of approximately 8–14 GHz in 7HP, 8–27 GHz in 8HP, and 11–37 GHz in 9HP. Fig. 18 shows a measured output of the VCO passed through a divide-by-16 circuit in 9HP. It has a period of 446 ps corresponding to 35.9-GHz output with the VCO control input at 1.25 V. The 9HP implementation utilizes a −2.5-V supply and consumes 59.5 mW of power. The unique interpolation technique creates much larger bandwidths than those achieved by other strategies in both SiGe and CMOS. It has the added advantage of not requiring carefully designed and large passives. Many other VCO implementations utilize LC tanks with varactor diodes or switchable passive elements to adjust frequency. These LC oscillators typically only contain one current tree, however, which saves power consumption.

A VCO with such large tuning range provides for much flexibility in a system, particularly in an adaptive RF front–end. Use of such an oscillator in conjunction with a Gilbert-cell-based frequency multiplier [34] can further extend the operating range and applications of such an oscillator in a single integrated solution. The FFI–VCO oscillator is suitable for use in a filtering system in conjunction with the ADC and FPGA, as discussed previously.

E. BiCMOS Crossbar Switch

In many systems, it is important to have a fast reconfigurable routing element. Routing within a network, sharing a bus line, or communicating across an array-structured system are all instances where speed plays a significant role in total system performance. A wideband SiGe crossbar switch could be used to reconfigure digital or analog cross connections in a variety of systems. We present here a crossbar switch design implemented in 8HP that is nonblocking and capable of 80-Gb/s transmission with a reconfiguration time of 160 ps [35]. With an 8 × 8 crosspoint configuration, the switch is capable of routing a possible eight inputs to eight outputs. A unique characteristic of the switch is that there is uniform delay along all paths to the output. This keeps data aligned and is achieved by utilizing a tree style data distribution network within the switch. Maintaining alignment of the inputs to the switch is especially valuable for applications in WDM systems or data serializers.

In this design, high-performance SiGe HBTs have been employed in circuitry along critical paths while FETs have been utilized along those less impactful and in those for configuration. To further reduce power consumption, an NFET switch is used as a current mirror in many of the CML trees. The ability to turn CML trees off allows the crossbar switch to power down unused paths through the NFET switch. If a particular application will not need the entire crossbar switch or if a path is simply waiting for an input, the unused portions of circuitry can be turned off.

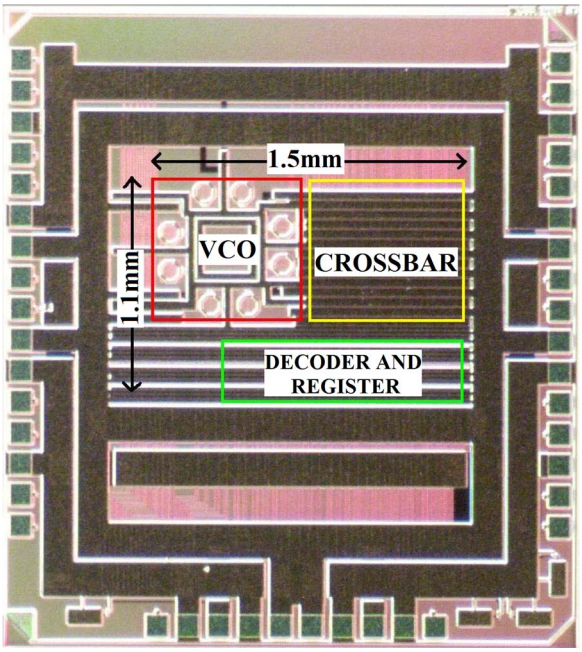

Fig. 19. *Micrograph of SiGe crossbar switch test die [35].*

Because of this, the crossbar switch can lower its power consumption from a maximum 5.7 W to 2.2 W from a −2.5-V supply depending on its configuration. Throughout the crossbar, high isolating BiCMOS cascode multiplexors are adopted. These multiplexors introduce another tier of transistors at the top of the current tree that prevent feedthrough of unwanted signals to an unintended output.

A test chip for the crossbar switch has been fabricated and is presented in Fig. 19. The crossbar occupies 1.65 mm^2 of space in the chip. To evaluate the performance of the crossbar the die has been configured as a phase router for a phased array system, as shown in Fig. 20. A 16-phase VCO is used to generate eight differential inputs to the crossbar switch while decoders and registers are used to select which output they are routed to. In this configuration, the crossbar is actually acting as a 16 × 8 switch due to each input handling two phases for the system. Output waveforms showing 38.8-GHz sine waves with selected phase are shown in Fig. 21. The level of performance achieved makes the crossbar switch well suited for applications in phased array antennas [36] and WDM systems. A 16 × 16 crosspoint switch has been reported utilizing a production AlGaAs/GaAs HBT process [37]. The switch was able to transmit at data rates up to 10 Gb/s while consuming 11.3 W. Another reported crosspoint switch in a 2 × 2 configuration in an InP process was shown to consume 0.9 W while transmitting at 25 Gb/s [16].

IV. FUTURE OF ULTRAFAST RECONFIGURABLE SYSTEMS

Current commercial SiGe technology is capable of cutoff frequencies as high as 300 GHz. Recently, Ning and Cai [38] proposed a lateral bipolar device in silicon that is capable of being integrated into an existing CMOS process

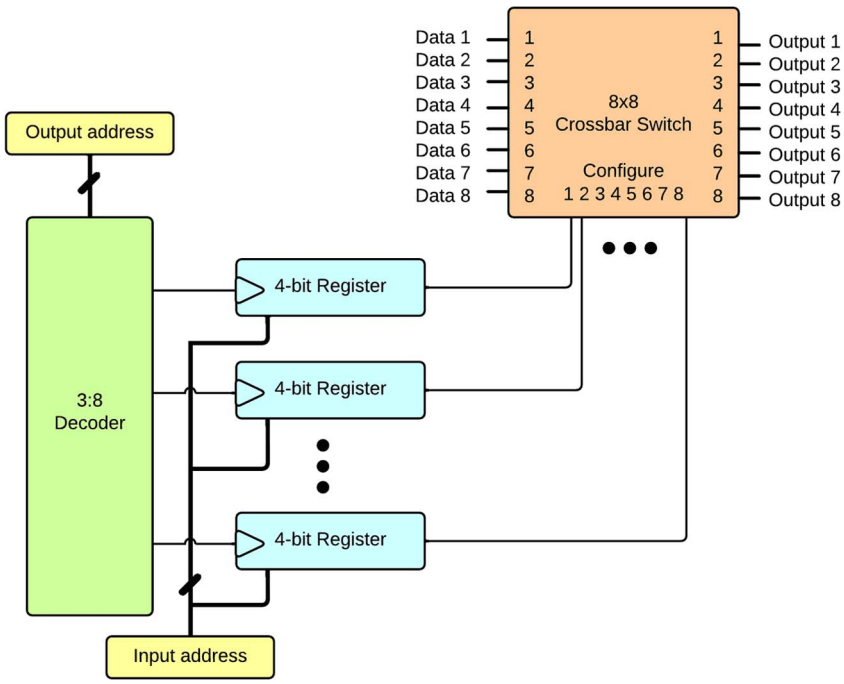

Fig. 20. *SiGe crossbar switch test die configuration.*

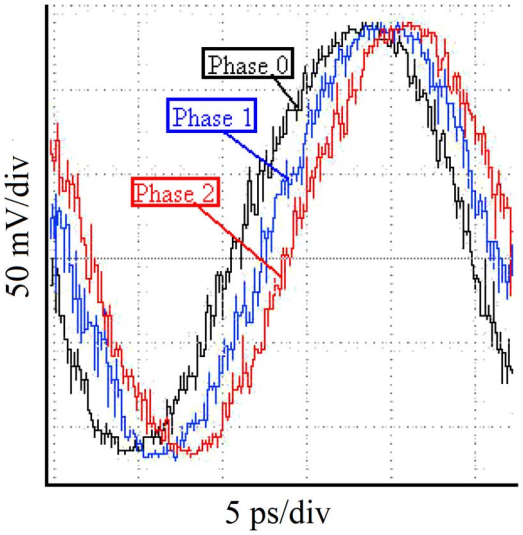

Fig. 21. *Output of crossbar switch test circuit corresponding to several selected outputs of the phased array system [35].*

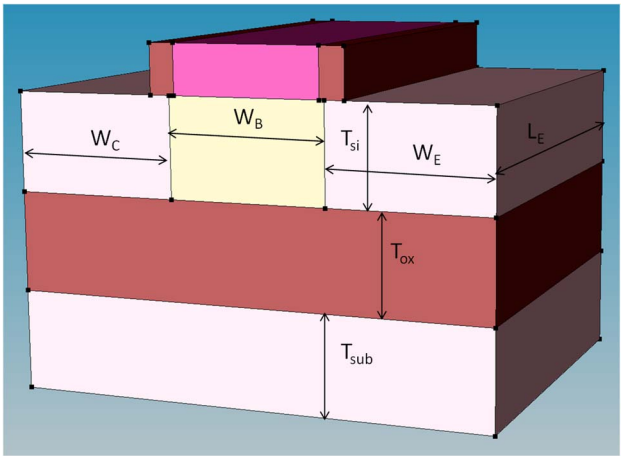

Fig. 22. *Device structure–lateral HBT (emitter, collector contacts on the left and right side faces, base contact on top of the extrinsic base).*

flow and can achieve very high cutoff frequencies with proper scaling. Cai *et al.* [39] fabricated NPN and PNP transistors on the same chip with a PD–SOI CMOS-compatible process flow using a standard CMOS mask set, which is not optimized for bipolar. Given the heavy investment in process infrastructure, this degree of CMOS process compatibility is critical for the adoption of any new device that shows promise at pushing the speed envelope. Table 3 shows the commonality in process flow for CMOS and the lateral bipolar device [40].

The lateral bipolar device is a symmetrical device, i.e., the emitter and collector regions of the device are identical in geometry and doping. This along with the fact that both NPN and PNP devices can be fabricated in the same process, allows us to revisit high-speed circuit design techniques like complimentary bipolar and current injection logic that were previously not feasible. A schematic illustration of the device is shown in Fig. 22. An added benefit of the device, because the base contacts are closer to the device, is that the density with which the device can be placed is greater than CMOS devices at the same lithography node. This is illustrated in Fig. 23. Any improvement in density has tremendous benefits in reconfigurable arrays such as FPGAs.

With essentially the same structure, variations of this device have been explored that optimize for power and speed. For instance, if the base of the device is fabricated from a material with a smaller bandgap than the material used for the emitter and the collector, the device can operate at a lower power level. On the other hand, if the base of the device is doped in such a way that it is partially depleted, the device can operate at a higher frequency at the expense of higher power. Modeled after experimental data from the 90-nm node, our simulations indicate that a device with SiGe base fabricated at 33-nm node would have a cutoff frequency of approximately 825 GHz and a maximum oscillation frequency of over 1 THz. As shown in Fig. 24, the collector current at cutoff frequency for such a

Table 3 Process Step Comparison [40]

CMOS	Lateral Bipolar
Well implant	Base implant
RTA	RTA
Gate dielectric	Permeable oxide
Gate electrode	Pre-doped polysilicon
Gate stack RIE	Oxide HM and gate RIE
Spacer 1	
Halo implant	
Spacer 2	Spacer
Source/drain implant	Emitter/collector implant
RTA	RTA
Silicide	Silicide

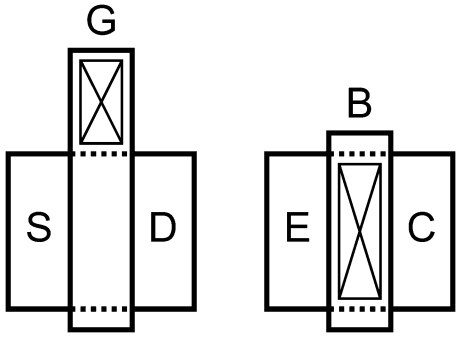

Fig. 23. *Layout for CMOS (left) and the lateral bipolar device (right). The ability to place the metal base contact on top of the base increases the density with which these devices can be placed. Adapted from [41].*

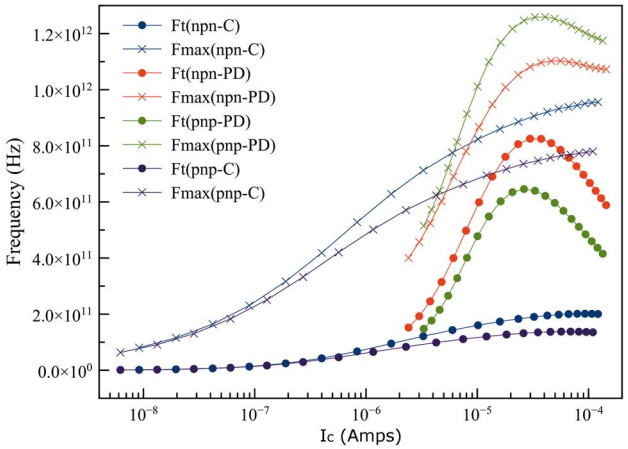

Fig. 24. ***f_t and f_{max} of NPN and PNP device with conventional base doping (C) and partially depleted base (PD).***

device (both NPN and PNP) is around 0.03 mA, roughly 100 times lower than commercial vertical HBTs.

With access to such a device, broadband terahertz electronics in a monolithic package, or terahertz monolithic microwave integrated circuits (TMICs), will become a reality. Future SiGe bipolar devices will provide the ability to generate, process, and transmit signals that currently no process is capable of. These bipolar transistors could be used to produce ultrafast communication links, in terahertz imaging, or to enhance spectroscopy. FPGAs will become an extremely compelling option for a far wider variety of applications. The improvements in speed and density would allow for FPGAs capable of emulating the most sophisticated ASICs or microprocessors while continuing to provide their trademark reconfigurability. With improved cutoff frequency, the power-performance tradeoff of the bipolar device can be employed much more aggressively. While the current bias at the peak f_T is already significantly reduced from that seen in the vertical HBTs, dropping the bias from the peak to match the application can then provide for an even larger reduction in power consumption.

V. CONCLUSION

In this paper, we describe how higher operating frequencies of ICs extend the applications of reconfigurable systems. We discussed the impact of these ultrafast reconfigurable systems across analog and digital domains. SiGe BiCMOS processes have been proposed as an ideal technology in which to build these systems. We presented several circuits designed in SiGe BiCMOS technology that expand the impact of reconfigurable systems. A high sample rate (80 Gs/s) 8-b ADC, 48 × 48 cell FPGA, 26-GHz tuning range VCO, and high-performance (80 Gb/s) crossbar switch all demonstrate the potential of high-speed circuits in reconfigurable systems. Fabricated implementations of several SiGe circuits described were presented. We have shown that each new generation of SiGe technology continues to obtain significant performance gain and that a new lateral bipolar device may provide for the largest boost yet. Future SiGe kits will be well suited for even more far reaching opportunities in designing ultrafast reconfigurable systems. ■

Acknowledgment

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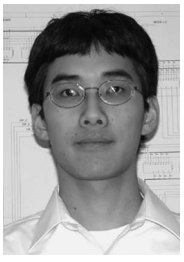

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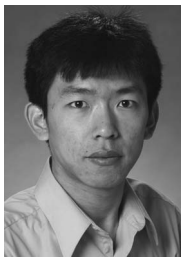

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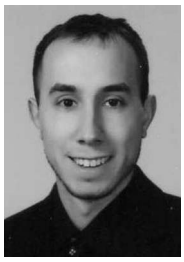

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