Measurement Methods and Applications to High-Performance Timing Test

Mani Soma
Univ of Washington, Seattle

Purpose
- To emphasize the measurement issues critical in high-frequency test
- To develop in-depth understanding of noise in measurements
  - timing noise, phase noise in RF systems
  - noise in converters
- To provide a foundation for research in RF measurement and test

Outline
- Top-down view of measurement issues
- Basic noise mechanisms and models
- Noise in measurement circuits
  - converters (sampled data)
  - PLL & VCO (clocks and data control)
- Case studies in measurement
  - existing methods and their noise considerations
- Research in measurement methods

System-level View
- Focus on measurements in RF systems

RF Test Requirements
- High-frequency test for specific blocks
  - RF digital blocks: PLL, I/O buffers
  - RF analog / mixed-signal blocks: transceiver, modulator, VCO, LNA, etc.
- Functional parametric test to verify performance
  - Phase, frequency, jitter, SNR, spectrum
- Automatic test
  - Role of low-frequency ATE

High-frequency Test Approaches
- Which measurement can be done most efficiently at high-frequency?
  - Voltage
  - Current
  - Time
- Which high-frequency measurement tool is available?
  - GHz clocks
  - Very fast sampler, converters
Focus on Measurement

- Measure = acquire raw data from a signal
  - usually taken for granted but …..
  - the critical first step of any test procedure
  - strong impact on final test accuracy and decision
  - strong impact in evaluating tradeoffs between on-chip and off-chip test

What Do We Measure?

- Voltage
  - capture signal points \( (t_n, V_n), n=1,N \)
  - S/H, ADC, and sampling clocks
  - most popular measurement methods
    - in oscilloscopes, spectrum analyzers, etc.
    - in ATE
  - post-processing
    - peak detection, voltage gain, amplitude, etc.
    - timing estimation (e.g. zero-crossing)
    - FFT: amplitude, phase, noise, etc.

What Do We Measure? (2)

- Current
  - capture current values (at one or a few points)
    - resistor, current sensor, clocks
  - implementation
    - built-in compliance in benchtop instrument
    - in ATE for IDDQ test
  - limited use
    - simple short/open detection
    - IDDQ, IDDI, IDDx testing for various faults
  - post-processing
    - usually for IDDQ applications

What Do We Measure? (3)

- Time and frequency
  - direct measurement by capturing signal edges
    - clocks for capturing edges
  - indirect measurement via FFT of voltage samples
  - recent strong interest in direct timing measurement
    - on-chip BIST
    - benchtop instrument (e.g. Wavecrest)
  - post-processing
    - FFT and/or statistical analysis

Measurement Issues

- No perfect measurement exists
- Limitations to accuracy
  - noise: fundamental limit
  - interactions between measuring instrument and circuit under test (CUT)
  - post-processing methods and interpretation of results

Outline

- Top-down view of measurement issues
- Basic noise mechanisms and models
- Noise in measurement circuits
  - converters (sampled data)
  - PLL & VCO (clocks and data control)
- Case studies in measurement
  - existing methods and their noise considerations
- Research in measurement methods
Noise Characteristics & Models

- Component noise and impact on measurement
  - Intrinsic noise
  - Both in CUT and in measurement circuits
- Timing noise of high-frequency circuits
  - Higher-level models
  - Measurement methods

Resistor Noise

- Thermal noise
  - Inherent ($T=0K$, $k=1.38E-23 J/0K$)
  - $1K\Omega$ @ $25^\circ C$ or $298^\circ K @ 1 MHz$ has $4\mu V$ noise

  \[ e_n^2 = 4kT R \Delta f \]

  \[ i_n^2 = 4kT \Delta f / R \]

Resistor Noise & Sampling Jitter

- Resistor noise creates timing uncertainty in input sampling
  - Need to design for at high frequencies
- Example
  - $50\Omega$ system, $10 MHz$ clock with $250 ps$ rise time
  - Noise-induced $2.7 ps$ jitter with $0.5V$ input

  \[ \Delta t_{CLK} = \frac{0.7 kT R_n}{f_{CLK} \sqrt{\pi \tau_{CLK}}} \]

Wiring Impact

- $16$-bit ADC on loadboard, $Z_\text{in} = 5K\Omega$, $5 cm$ of PCB copper track ($0.25 \text{ mm}$ wide, $0.038 \text{ mm}$ thick) between input and signal source
- $R$ (wire) = $0.09 \Omega$
- Gain error = $R / Z_\text{in} = 0.0018\%$ (> $0.0015\%$ = LSB for $16$ bits)
- Data accuracy is no longer $16$-bit!!

Other Resistor's Parasitics

- Skin effects ($f > 10 MHz$ for high resolution converters and high-frequency clocks)
- Copper (on PCB or on chip)

  \[ \text{Skin depth}(cm) = 6.6 / \sqrt{f(\text{Hz})} \]

  \[ R_{\text{square}}(\Omega) = 2.6 \times 10^{-7} \sqrt{f(\text{Hz})} \]

Resistive Noise Reduction Methods

- Reduce noise in design
  - Use differential designs
  - Match layout
  - Model and simulate with noise sources, series inductance and parallel capacitance
- Reduce noise in measurement
  - Use shielding or guard
  - Use differential measurement circuits
  - Use low-valued resistors
  - Reduce measurement bandwidth if possible
  - Use averaging methods in voltage measurement
Noise in Capacitors

- Capacitance between parallel wires -> crosstalk
- Capacitance between bond wires (~ 0.2 pF)
- Capacitor intrinsic noise
  - 1 pF @25°C has 64 µV noise
  
  \[ e_n(C) = \sqrt{\frac{kT}{C}} \]

Capacitor Models in Measurement

- Use different models depending on measurement applications
- Add noise models for each component

  ![Model Diagrams]

Shot noise

- Discrete nature of current flow
- Shot noise current
  - \( q = 1.602 \times 10^{-19} \) C
  - another type of white noise

  \[ I_n^2 = 4qI_{DC}\Delta f \]

1/f noise

- Flicker noise (terminology from vacuum tube)
  - generally 1/f, \( \alpha = 0.8 - 1.3 \)
  - very common
- Many names
  - excess noise, pink noise, contact noise, etc.
  - burst noise (popcorn noise): 1/F, \( \alpha = 1 - 2 \), usually 2
- red noise: 1/F
- Spectral density

  \[ S_n(f) = \frac{E_n^2}{f} \]

Noise bandwidth

- Noise bandwidth ≠ 3-dB bandwidth
  - usually larger than 3-dB bandwidth
- Definition
  - system with voltage gain \( A_v(f) \) or power gain \( A_p(f) \),
    maximum gain = \( A_v0 \)

  \[ \Delta f = \frac{1}{A_v0} \int |A_v(f)|^2 df \]
- First-order lowpass filter example
  - 3-dB bandwidth = \( f_L \)
  - noise bandwidth = \( \pi f_L / 2 \)
Note on measurement

- White (thermal) noise
  - longer measurement time reduces noise impact
  - accuracy increases as $T_{\text{measure}}^{1/2}$
- 1/f noise
  - measurement accuracy does not increase with measurement time
- Burst noise
  - amplitude and frequency (# bursts/sec)
  - need bandwidth large enough to capture sudden short burst, small enough to avoid thermal noise dominance

“Ground” in measurement

- realistic ground (ground loop)

Other ground loops

- Current from one source flows through ground impedance of the other source
- Current around ground loop creates magnetic coupling

Dealing with ground loops

- Guidelines for both design and test
- Separate digital and analog power and ground
- Join grounds at one point of the device

Signal routing guidelines

- Separate analog and digital signals
- Avoid crossovers between analog and digital signals
- Layout sampling clock and analog input wires carefully
- Layout high-impedance signals carefully
- Use differential designs

Noise in test set-up

- Instruments, ATE, on-chip test circuits all have noise
  - fundamental limit to measurement accuracy
  - system noise floor
    - highly dependent on test set-up
    - no industry standard for interpretation
    - need to understand basic mechanisms to interpret measurement and test results
System noise components

- Random noise
  - random timing jitter of test clocks
  - thermal noise
- Digital crosstalk and clock / signal harmonics
  - distinct spikes in spectrum
  - correlated to analog input or clock
  - synchronized noise
- Other noise sources
  - broad “needles” in spectrum
  - switching power supplies, linear power supplies, switching signals
  - non-synchronized

Case study: System noise

- Use ADC to characterize system noise
- Ideal 16-bit ADC
  - SNR (dB) = 6.02*16 + 1.76 = 98.08 dB
  - SNR = SQDR: noise includes quantization distortion, dynamic non-linearities, internal jitter, and internal thermal noise
- Measure via coherent sampling
  - larger sample size -> noise spread over more samples
  - noise per FFT bin decreases
  - noise improving figure NIF with N=2^K samples
  
  \[ NIF(dB) = 10 \log \frac{N}{2} = 3.01(K - 1) \]

Noise floor calculations

- 16-bit ADC, 2^{17} samples
  - SQDR = 98.08 dB, NIF = 48.16 dB
  - noise floor (dBc) = SQDR+NIF = 146.24 dB
- noise floor (mean and absolute values)
  - signal swing: -5V to +5V
  - signal amplitude: 5V or 20 log 5 = 13.98 dBV
  - mean noise floor (dBV) = 146.24 - 13.98 = 132.26 dB
  - absolute noise floor (dBV) = 132.26 - 11 = 121.26 dB
  - > 11 dB: worst-case bin 11 dB greater than mean bin, due to Gaussian distribution of quantization noise

Sample size vs. noise floor

- Small number of samples: noise floor not visible
  - SQDR+NIF
  - Noise floor due to quantization distortion

Sample size vs. noise floor (2)

- Larger number of samples: noise floor components and spurious component
  - SFDR = spurious-free dynamic range

Case study: experiment

- Analogic ADC 4355
- Input signal frequency \( f_s = 997.162 \text{ Hz} \) (approx. 1 KHz)
- Sampling frequency \( f_s = 100000.0135 \text{ Hz} \) (approx. 100 KHz)
  - Nyquist bandwidth = 50 KHz
  - Number of signal periods = 1307
  - Record size = 131072 samples = 2^{17}
  - FFT frequency resolution = 100 KHz/2^{17} = 0.763 Hz
What type of sampling?
- From the spectrum, is the sampling coherent? Accurate? Why?
- Is the sampling clock jitter-free? Why?

Harmonics and spurious noise
- Is the spike at 11.965 KHz a signal harmonic or spurious noise?

Harmonics and spurious noise (2)
- Is the spike at 27.491 KHz a signal harmonic or spurious noise?

Answers
- \( f_i \) (signal) = 997.162 Hz
- \( f_s \) (sampling) = 100000.0135 Hz
- \( f = 11.9659 \) KHz = 12 \( \times \) 997.162 Hz = 12th harmonic
- \( f = 27.491 \) KHz = 2\( \times \)\( f_s \) - 173\( \times \)\( f_i \) = 173th harmonic folded back into the Nyquist band

Harmonics identification
- Higher harmonics folded back into the Nyquist band
- \( n \) = frequency zone
  - zone 0: 0 - 0.5 \( f_s \) (Nyquist band)
  - zone 1: 0.5 \( f_s \) - \( f_s \)
  - zone 2: 1.5 \( f_s \) - 2 \( f_s \)
- \( M \) = \( M \)th harmonic of signal (\( M = 1, 2, 3 \ldots \))
- \( f \) (\( M \)th harmonic in zone \( n \) folded to Nyquist zone) = \( (n \times f_s + M \times f_i) \) or \( (n \times f_s - M \times f_i) \)

Harmonics and signal
- Given input frequency \( f_i \) and sampling frequency \( f_s \), identify harmonic bin \( f_h \)
  - \( i \) = largest integer \( \leq 2 \frac{f_i}{f_s} \)
  - \( \frac{f_i}{f_s} = (1 - \frac{1}{2}) \left( f_s - \left( i + \frac{1 - (-1)^i}{2} \right) \frac{f_s}{2} \right) \)
- Given a peak frequency \( f_p \) and sampling frequency \( f_s \), identify signal frequency \( f_i \)
  - \( i = 0, 1, 2, 3 \ldots \) (ambiguity in identification)
  - need 2 sampling rates to identify better
  - \( f_i = (1 - \frac{1}{2}) \left( f_s - \left( i + \frac{1 - (-1)^i}{2} \right) \frac{f_s}{2} \right) \)
**Outline**
- Top-down view of measurement issues
- Basic noise mechanisms and models
- Noise in measurement circuits
  - converters (sampled data)
  - PLL & VCO (clocks and data control)
- Case studies in measurement
  - existing methods and their noise considerations
- Research in measurement methods

**Noise calculation in converters**
- DAC
  - ground all digital inputs
  - place noise sources (thermal, shot, 1/f, etc.) in appropriate circuit elements
  - contributions from each noise source type
    - resistor, opamp, input voltage noise, input current noise
  - calculate total noise using circuit analysis
    - sum independent noise power

**DAC R-2R network noise**
- Total noise spectral density
  - independent of N
  - $E_{n}^2 = 4kTR$

**DAC binary-weighted network**
- Total spectral density
  - approximately $E_{n}^2 = 2kTR$

**DAC topologies vs. noise**
- 4 topologies
  - R-2R with voltage follower
  - R-2R with inverting amplifier
  - R-2R with non-inverting amplifier
  - Binary-weighted with inverting summer
- Which has lower total noise at output?
- Why?
DAC noise analysis

- Normalizing assumptions
  - to make noise transfer function = 1 in all topologies
  - R-2R networks: $R_L = R_1 = R_2 = R$
  - binary-weighted network: $R_F = R_{eq} = R/2$
- Lowest noise
  - R-2R with follower (fewest components, no multiplication of opamp noise due to gain=1)
  - binary-weighted could be better if amplifier noise dominates

DAC noise lessons

- Use amplifier with lowest noise
  - $E_n$ of amplifier dominates DAC noise
- Use low-noise reference voltage
  - second dominant noise factor
- Binary-weighted DAC
  - below 1 KHz: resistor 1/f noise dominates
  - above 1 KHz: voltage reference noise dominates

ADC noise model

- Flash ADC example
- Noise components
  - resistor noise
  - reference noise
  - comparator noise (voltage and current)
- Noise models: white and 1/f
- Ignore digital encoder noise

ADC noise analysis

- largest contribution of $V_{ref}$ noise
- all other sources contribute
- most noise at the mid-range comparators

ADC noise vs. bit error

- Noise distribution with respect to LSB quantization window
  - Gaussian
  - center of each quantized step
- $6\sigma$ spread of the noise distribution
  - within quantization step: no bit error
  - outside quantization step
    - calculate probability of one-bit error

Outline

- Top-down view of measurement issues
- Basic noise mechanisms and models
- Noise in measurement circuits
  - converters (sampled data)
  - PLL & VCO (clocks and data control)
- Case studies in measurement
  - existing methods and their noise considerations
- Research in measurement methods
Phase noise and timing jitter

- Two domains to characterize clocks in measurement
  - Timing systems: jitter
  - RF systems: phase noise
  - How to relate them?
- Case study: VCO and other oscillators
  - $S_\phi(\omega)$ = phase noise in dBc (reference to carrier at $\omega_0$) at the offset frequency $(\omega - \omega_0)$ from the carrier
  - $J_{cc, RMS}$ = RMS value of cycle-to-cycle jitter
  - White noise sources (thermal and shot noise)

$S_\phi(\omega) = \frac{a_0^2 / 4 \pi^2 f_0^3}{(\omega - \omega_0)^2}$

$J_{cc, RMS}^2 = \frac{4 \pi}{a_0^2} S_\phi(\omega) (\omega - \omega_0)^2$

Noise and timing jitter (1)

- VCO with supply and substrate noise
  - Non-white noise: model by noise modulation $V_m \cos(\omega_m t)$
  - RMS value of period jitter $J_{P, RMS}$ increases with noise amplitude
  - RMS value of cycle-to-cycle jitter $J_{cc, RMS}$ increases with noise frequency

$J_{P, RMS} = \frac{V_m K_{VCO}}{2 f_0}$

$J_{cc, RMS} = \frac{V_m K_{VCO}}{f_0} \frac{1 - \cos(\omega_m / f_0)}{2 f_0} \approx \frac{V_m K_{VCO}}{2 f_0^3}$

Noise and timing jitter (2)

- Single-ended VCO
  - Supply and substrate noise
  - $V_m = \Delta V_{DD} = 100$ mV
  - Analytical vs. simulated results

Noise and timing jitter (3)

- Differential-ring VCO
  - Supply and substrate noise
  - $V_m = \Delta V_{DD} = 100$ mV
  - Analytical vs. simulated results

Measurement guidelines

- Spectrum analyzer
  - More noise measured with higher bandwidth
    - Cannot be compared directly
    - Divide each noise measurement by $(\Delta f)^{1/2}$ for comparison
  - Analyzer calibrated resolution bandwidth ≠ noise bandwidth
  - Need to know how to interpret measured data correctly
### Measurement time

- Instrument response time: \( \tau \)
  - Smallest time window possible
- Measurement bandwidth: \( \Delta f \)
- Relative error:
  \[
  \varepsilon = \frac{1}{\sqrt{2\pi \Delta f}}
  \]
- Use widest possible bandwidth (see next slide)
  - Narrowband measurements require more averaging for same accuracy
- Use long time window (with averaging when appropriate)

### Noise reduction in measurement

- Use measurement methods with differential circuits and signals
- Use smaller bandwidth
  - Just "enough" bandwidth to reduce noise and still get good accuracy (previous slide)
- Employ signal separation and shielding
- Reduce transition switching in the measurement circuits
  - Use current-steering methods in analog measurement circuits to avoid \( di/dt \) transient

### Noise reduction in measurement (2)

- "Instrument" = ATE, external instrument, or on-chip measurement circuit
- Considerations for sub-ps timing measurements
  - DUT - instrument interface
  - Instrument one-shot resolution / accuracy
  - Instrument DC input accuracy
  - Instrument physical location relative to DUT
  - Instrument jitter noise floor
  - Instrument throughput over data interface
  - Instrument trigger mode
  - Instrument bandwidth required to measure DUT timing parameters (rise, fall, delay, etc.)

### Outline

- Top-down view of measurement issues
- Basic noise mechanisms and models
- Noise in measurement circuits
  - Converters (sampled data)
  - PLL & VCO (clocks and data control)
- Case studies in measurement
  - Existing methods and their noise considerations
- Research in measurement methods

### Measuring Voltage: Sampling

- Signal under test
- Sample-and-Hold (SH)
- Digitizer (ADC)
- Memory storage
  - CLK

### Sampling Architecture

- ATE
  - Control protocols
- Clock sources
  - DC references
- Memory Analysis
  - Extraction
- ADC & temporary registers
- Customer IC
  - Test controller

Consider noise floor of entire test set-up, including on-chip measurement circuits
Sampling Clock Issues

- Frequency
  - On-chip: limited by technology (CMOS, SiGe CMOS, BiCMOS)
    - 2 - 5 GHz
    - same speed as fastest on-chip signals
  - ATE: 1 GHz
    - limited by pin electronics and test setup
  - Benchtop instrument
    - up to 40 GHz samplers

Faster Sampling Methods

- Delay-line interpolation
  - on-chip or ATE
  - 1 GHz clock + 7-stage delay line (125 ps each) = 8 GHz sampling clock

Faster Sampling Methods (2)

- Parallel samplers
  - ATE and benchtop instruments
  - up to 40 GHz sampling rate

Sampling Limitations

- Clock jitter
  - signal with 100-ps rise time
  - sampled with 5-ps jitter clock
  - 5% error in sampled values
    - averaging to reduce error in periodic signals
    - no correction for one-shot signal

Sampling Limitations (2)

- Clock synchronization
  - synchronized with signal to be sampled
  - synchronized between sampling clocks

Realistic clock jitter values

- On-chip (CMOS / BiCMOS) as of 2002:
  - 2.2 GHz - 6 GHz clocks
    - 30 - 40 ps peak-to-peak jitter
    - 3 - 5 ps RMS jitter

- Off-chip
  - ATE, oscilloscope, spectrum analyzer, TIA
    - 1 - 10 ps RMS jitter
    - 200 fs resolution with 2 ps noise floor (best case)
    - need calibration before measurements
Sampling Limitations (3)

- Undersampling is better?
  - Lower-frequency more stable clocks
  - Fundamental problems in time coherency

![Diagram](https://via.placeholder.com/150)

Measuring Voltage: Sampling

Sampling Limitations (4)

- Sample-and-Hold (capacitor noise, opamp noise, switching noise)
  - limited bandwidth
  - aperture error
  - transient response, overshoot, etc.
- ADC (noise estimation from previous slides)
  - sample rates at 8-bit < 400 MHz
  - parallel (4-channel) ADC: synchronization error
    - ATE or benchtop instrument only
- Memory storage
  - limited on-chip memory or temporary buffer

Sampling noise sources

- Uncorrelated noise
  - thermal noise
  - 1/f noise
- Correlated noise (difficult to estimate correlation)
  - power supply noise
  - substrate noise
  - clock synchronization noise
    - delay-line generation of clocks, parallel clocks
- Noise floor of the on-chip measurement circuit
  - in dB for amplitude sampling
  - in ps for timing accuracy

Direct Digital Conversion

- Sigma-delta modulator
  - pulse-density conversion method
  - low frequency and low conversion rates

![Diagram](https://via.placeholder.com/150)

Method limitations

- Clock jitter
- Jitter in output signal edges
  - need to characterize for each modulator design
- Post-processing issues
  - what parameters to extract from pulse stream?
    - on-chip or off-chip extraction
    - corruption / modulation of signal edges during processing due to jitter and noise sources
  - correlation to accepted measurements
    - phase noise, frequency, timing parameters
Measuring Current on ATE

- VS2
- Tester Channel #2
- Loadboard
- Circuit Under Test
- Tester Channel #1
- VS1
- Supply noise
- Resistive noise
- Current shot noise
- Supply noise

Measuring Current on Chip

- Vdd
- BIC Sensor
- GND

Current Measurement Issues

- Slow measurement
  - ATE: 100 µs - 3 ms; BICS: 50 µs - 500 µs
- Lower accuracy than voltage measurement
- Effects on on-chip VDD and GND
  - Power supply values reduced due to sensors
  - Power supply noise and ground noise increase

Current measurement noise sources

- Uncorrelated noise
  - Thermal noise
  - 1/f noise
  - Shot noise
- Correlated noise
  - Power supply noise
  - Substrate noise
- On-chip comparator noise
  - Reference noise
  - Comparator offset and input noise

Methods to Measure Time

- Sampling
  - Indirect method, already covered
- Counter-based method
- Time-to-voltage converter
- Time-to-digital converter
- Differential oscillator method
- Delay search method
- Start-and-stop counter method

Counter-based Method

- Time interval much larger than $T_{CLK}$
- Resolution = 1 clock period $T_{CLK}$
  - Improved by delay-line interpolation

Soma 14
Counter-method Observations

- All-digital circuits
  - more robust and scalable with processes
  - accuracy can be improved
  - easier on-chip circuit designs
- Key noise is clock jitter
- Need modifications if the time interval to be measured is < $T_{\text{min}}$ of fastest signals
- The core of many subsequent techniques

Time-to-Voltage Converter

- Need a DC voltage measurement or Pass / Fail comparison
- Requires analog components
  - sources of errors
- Measurement time
  - $T+$ pre-charge time

\[ V = V_{DD} - \frac{I_T}{C} \]

Time-to-Digital Converter

- Delay-line method to search for a signal edge
- Resolution = 1 unit delay
- Robust and very popular

Differential-Oscillator Method

- Measure a time interval $T$
  - Credence, Vector12
- Resolution = 1 unit delay
  - may be used to search for a signal edge

\[ T = m_1 T_1 - m_2 T_2 \]

Differential-Oscillator Method (2)

- Measurement time depends on edge coincidence
  - coarse / fine tuning options
  - may miss many edges in a periodic signal
  - no cycle-to-cycle measurement
- Clock-triggering mechanisms and errors
- Jitter on measuring clocks CLK1, CLK2
  - may be correlated
- Noise and error in coincidence detector

Delay Search Method

- Adjust Capture CLK to measure delay
  - absolute value or Pass / Fail
  - may be used to search for a signal edge
- Resolution in the ps range for on-chip test
Start-Stop Counter Method

\[ T_{average} = m_{CLK} T_{CLK} / N_{signal \text{-edges}} \]

Start-Stop Method Observations

- Variations of basic counter methods
- Start clock to count at one signal edge and stop count at another predetermined signal edge
- Mostly digital designs
- Same issues with other counter-based methods
- Additional problem due to re-triggering after stop
  - dead-time interval
- Core of Wavecrest timing analyzer

Outline

- Top-down view of measurement issues
- Basic noise mechanisms and models
- Noise in measurement circuits
  - converters (sampled data)
  - PLL & VCO (clocks and data control)
- Case studies in measurement
  - existing methods and their noise considerations
  - Research in measurement methods

Sampling Research

- Sampling in the presence of both voltage noise and timing jitter
  - theory and noise analysis
  - new sampling and post-processing methods
- Undersampling research with low timing coherency
  - critical for on-chip RF test
- Fast clocks for Nyquist sampling

Current-measurement Research

- Faster methods to measure currents
- Higher measurement resolution
  - at lower VDD
- Better designs of BICS to reduce noise effects on power supply and GND
  - critical for on-chip test
- More post-processing theory and methods
  - comparable to voltage sampling

Timing-measurement Research

- Theory and methods to reduce impact of jitter and timing noise in measurement
- Fundamental understanding of physical effects in turning ON / OFF transistors
  - critical to controlling clock edges
  - critical also to sampling and current-based methods
- Better circuits to capture timing edges
  - process variations
Leaping toward the Unknown

- Continuous-time measurements possible?
  - all current methods capture discrete values or edges, not waveform segments
  - no Sample-and-Hold
- Get rid of switches in measurement circuits?
  - no timing uncertainty
- Processing analog values directly?
  - no ADC, no clocks, no switches

Conclusion

- Noise models of basic components in on-chip design-for-test circuits
- Noise of measurement circuits and their impact on accuracy
  - noise source identification from measured data
  - noise components in each measurement method
- Guidelines for low-noise measurements
- Suggested research problems