

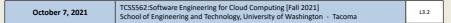
Wes J. Lloyd School of Engineering and Technology University of Washington - Tacoma



OBJECTIVES - 10/7

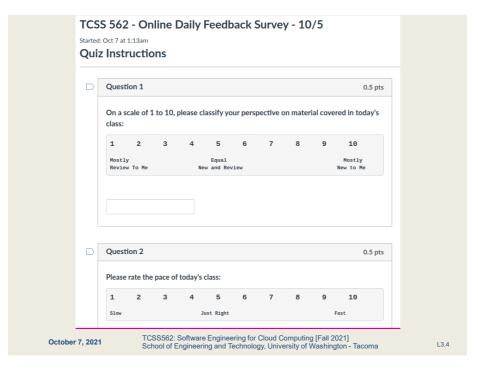
Questions from 10/5

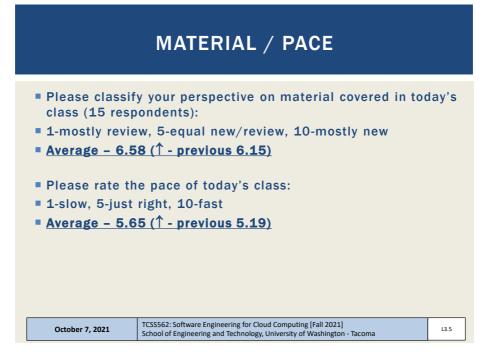
- Tutorial 2 Introduction to Bash Scripting
- Class Activity 1 Implicit vs Explicit Parallelism
- SIMD architectures, vector processing, multimedia extensions
- Graphics processing units
- Speed-up, Amdahl's Law, Scaled Speedup
- Properties of distributed systems
- Modularity
- Introduction to Cloud Computing –based on book #1: Cloud Computing Concepts, Technology & Architecture

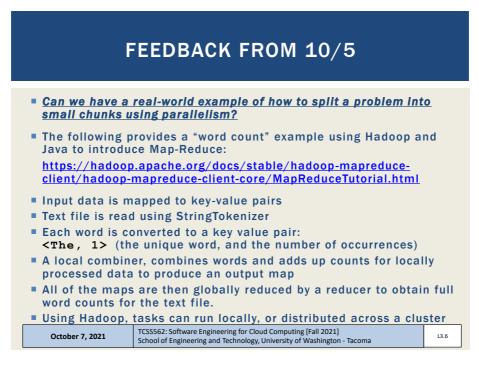


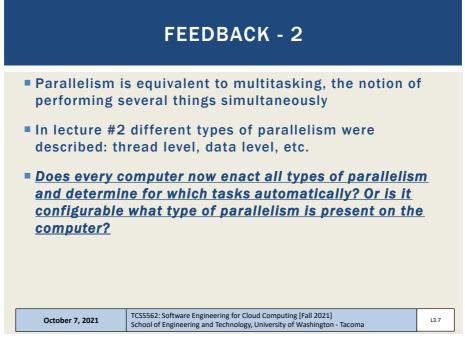


ONLIN	E DAILY F	EEDBACK SURVEY	
 Daily Feedbac Extra Credit for completing 	Announcements	as - Take After Each Class Upcoming Assignments Class Activity 1 - Implicit vs. Explicit Parallelism Available until Oct 11 at 11:59pm Due Oct 7 at 7:30pm -/10 pts Tutorial 1 - Linux Available until Oct 19 at 11:59pm Due Oct 15 at 11:59pm -/20 pts Past Assignments TCSS 562 - Online Daily Feedback Survey - 10/5 Available until Dec 18 at 11:59pm Due Oct 4 at 8:59pm -/1 pts TCSS 562 - Online Daily Feedback Survey - 9/30 Available until Dec 18 at 11:59pm Due Oct 4 at 8:59pm -/1 pts	
October 7, 2021		ing for Cloud Computing [Fall 2021] echnology, University of Washington - Tacoma	L3.3









	Available ?	Automatic ?
Thread-Level Parallelism (TLP)		
Data-Level Parallelism (DLP)		
Bit-Level Parallelism		
Instruction-Level Parallelism		

	Available ?	Automatic ?			
Thread-Level Parallelism (TLP)	YES	NO Programmer implements threads			
Data-Level Parallelism (DLP)					
Bit-Level Parallelis	n				
Instruction-Level Parallelism					
¹ - see: https://en.wikipedia.org/wiki/Streaming_SIMD_Extensions					
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AVAILABLE ON X86 CPUS				
		Available ?	Automatic	?
Thread-Level Parallelism (TLP)		YES	NO Programmer implements	threads
Data-Level Parallelism (DLP)		YES ¹ But only available when using special extensions (e.g. SIMD instructions)	NO Programmer impler code to use DLP fea	
Bit-Level Parallelism				
Instruction-Level Parallelism				
¹ - see: https://en.wikipedia.org/wiki/Streaming_SIMD_Extensions				
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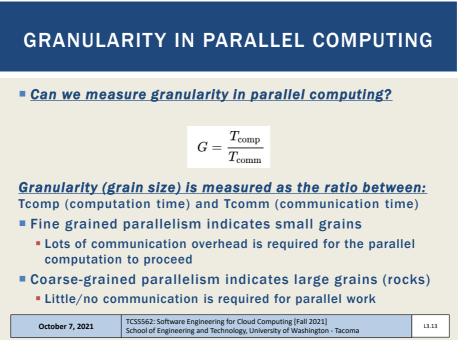
AVAILABLE ON X86 CPUS

	Available ?	Automatic ?	
Thread-Level Parallelism (TLP)	YES	NO Programmer implements threads	
Data-Level Parallelism (DLP)	YES ¹ But only available when using special extensions (e.g. SIMD instructions)	NO Programmer implements code to use DLP features	
Bit-Level Parallelism	YES	YES	
Instruction-Level Parallelism			
¹ - see: https://en.wikipedia.org/wiki/Streaming_SIMD_Extensions			

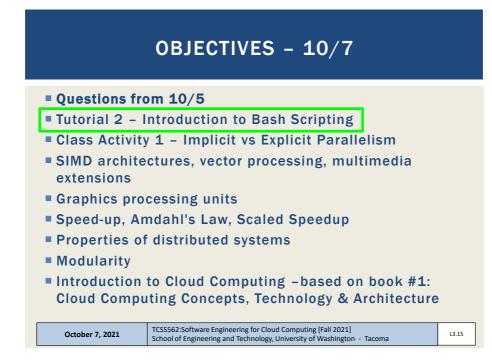
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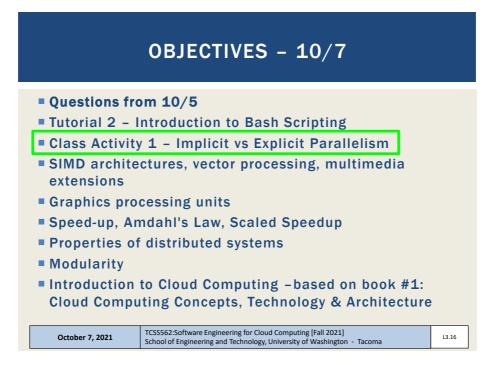
AVAILABLE ON X86 CPUS				
	Available ?	Automatic ?		
Thread-Level Parallelism (TLP)	YES	NO Programmer implements threads		
Data-Level Parallelism (DLP)	YES ¹ But only available when using special extensions (e.g. SIMD instructions)	NO Programmer implements code to use DLP features		
Bit-Level Parallelism	YES	YES		
Instruction-Level Parallelism	YES	YES		
¹ - see: https://en.wiki	pedia.org/wiki/Streamir	ng_SIMD_Extensions		

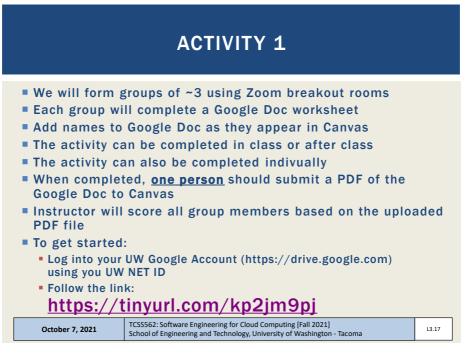
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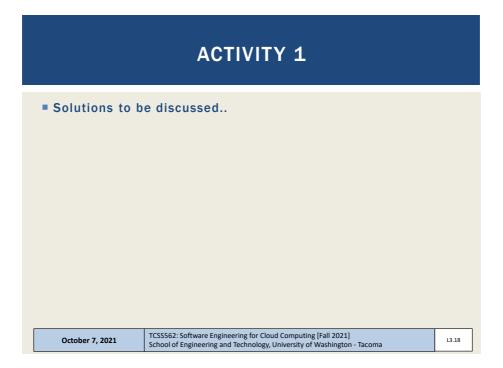


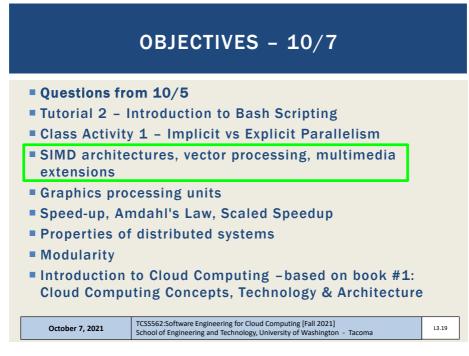


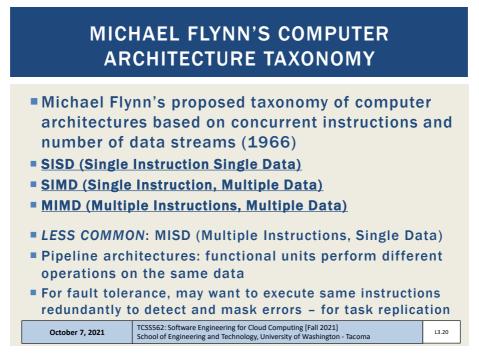


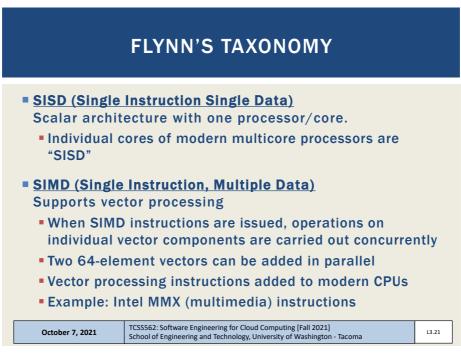


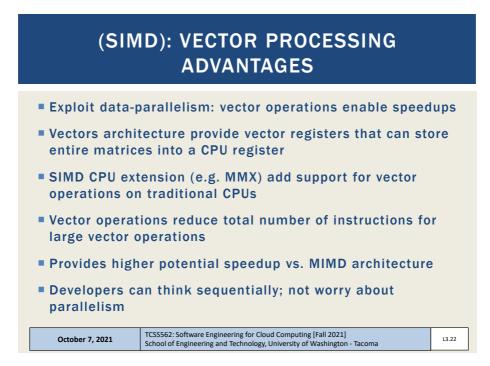


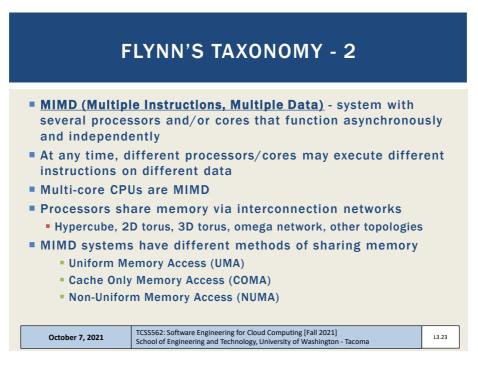


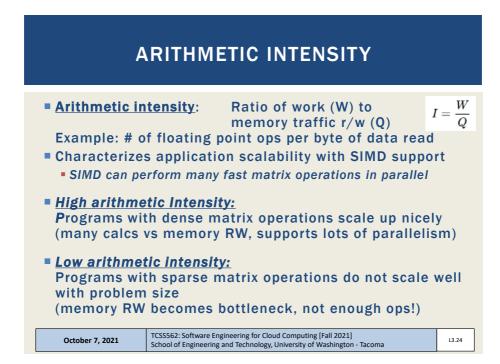


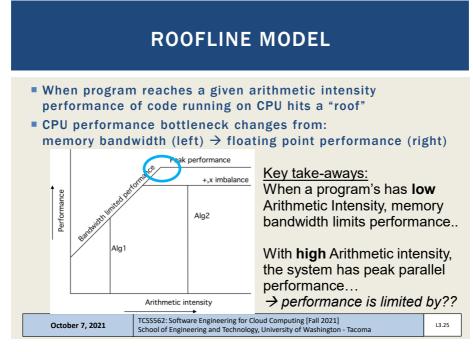


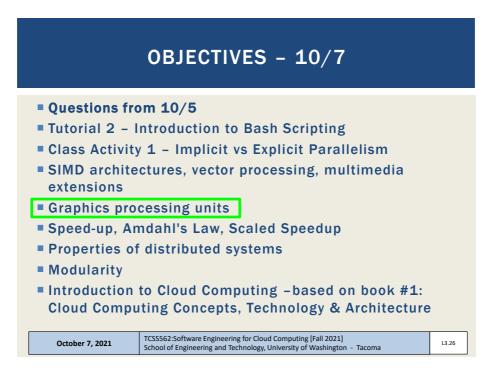












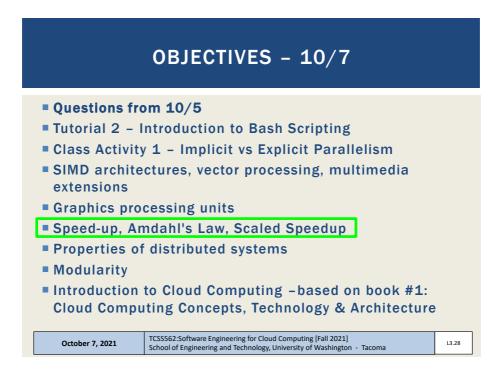
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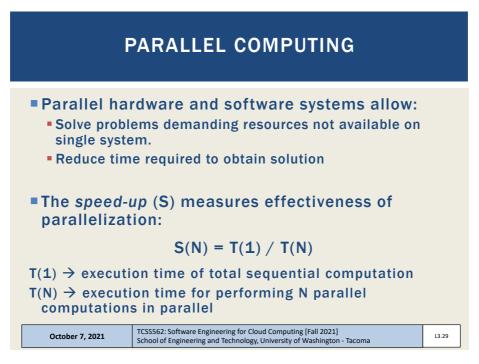


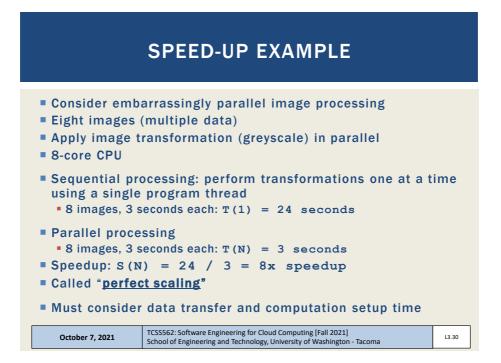


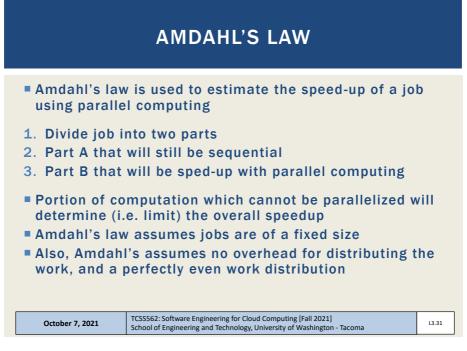
- Typically 7 to 15 SIMD processors each
- 32,768 total registers, divided into 16 lanes (2048 registers each)
- GPU programming model: single instruction, multiple thread
- Programmed using CUDA- C like programming language by NVIDIA for GPUs
- CUDA threads single thread associated with each data element (e.g. vector or matrix)
- Thousands of threads run concurrently

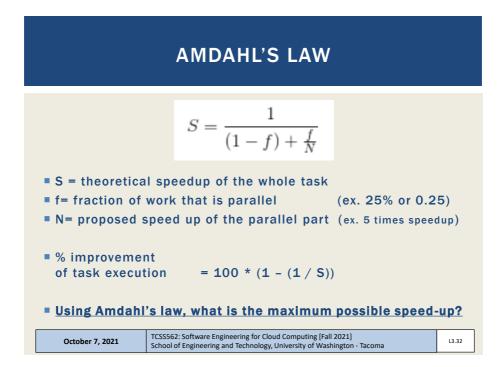
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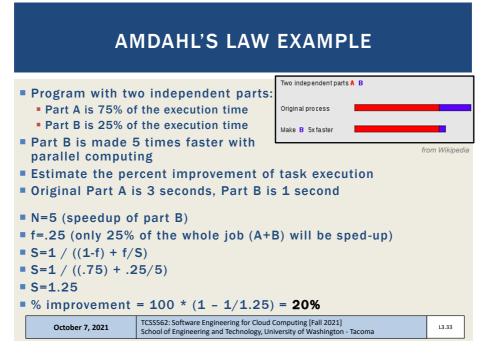


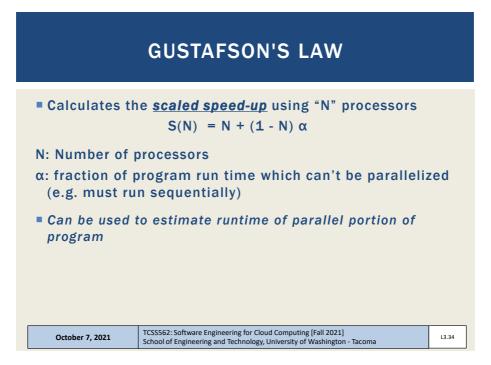


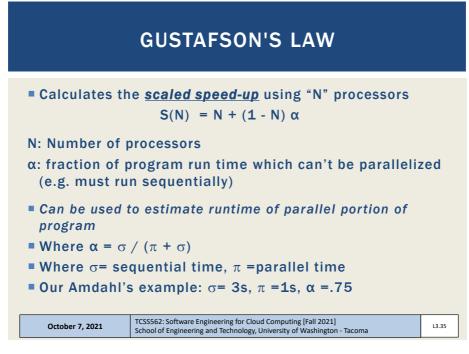


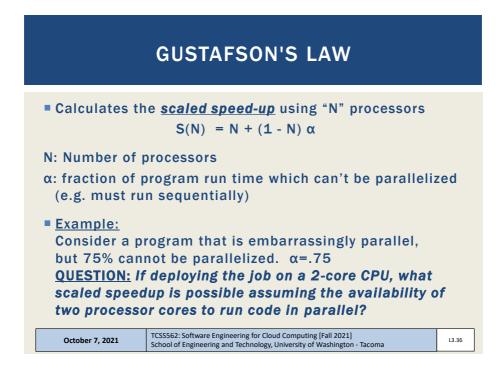


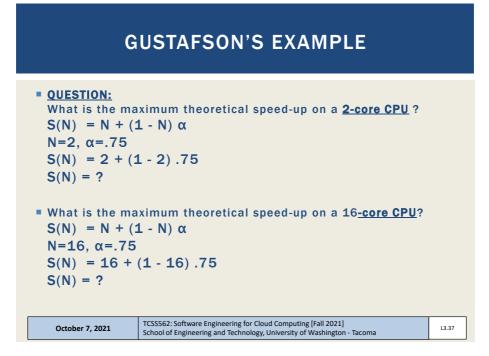


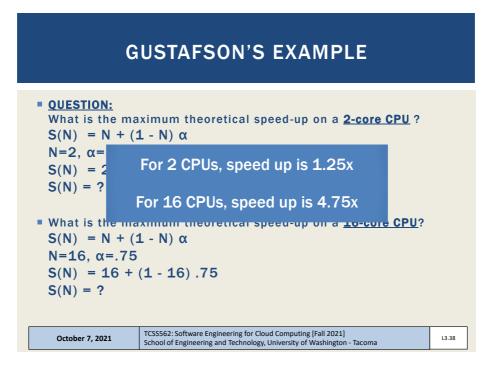


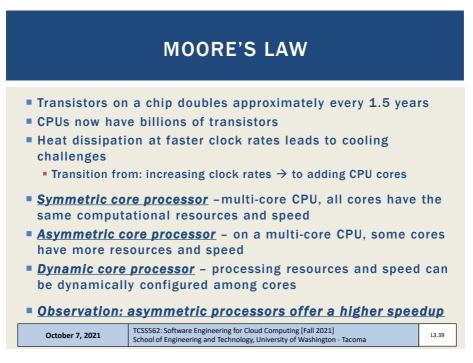


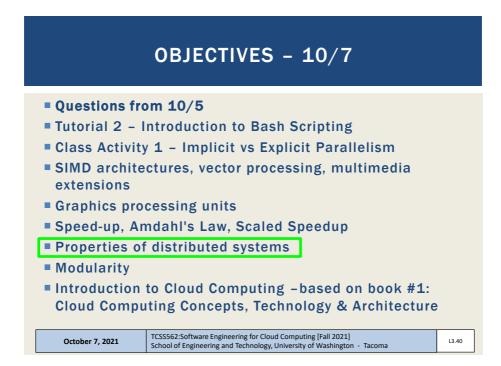






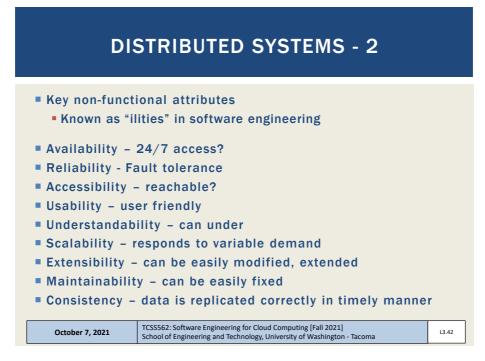


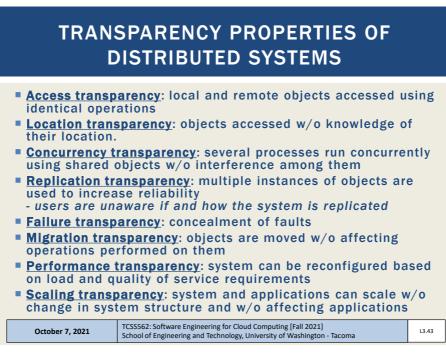




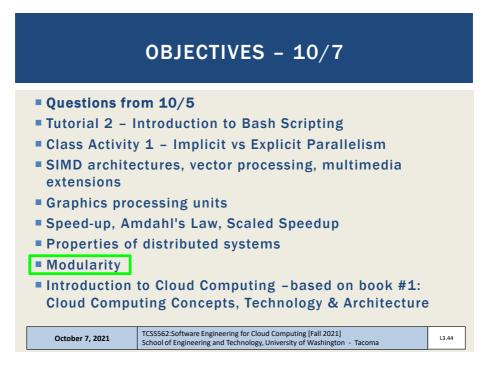


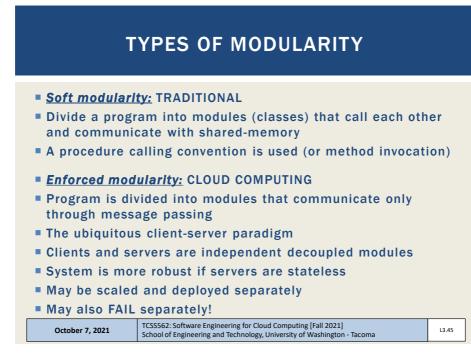
- Collection of autonomous computers, connected through a network with distribution software called "middleware" that enables coordination of activities and sharing of resources
- Key characteristics:
- Users perceive system as a single, integrated computing facility.
- Compute nodes are autonomous
- Scheduling, resource management, and security implemented by every node
- Multiple points of control and failure
- Nodes may not be accessible at all times
- System can be scaled by adding additional nodes
- October 7, 2021
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 L3.41

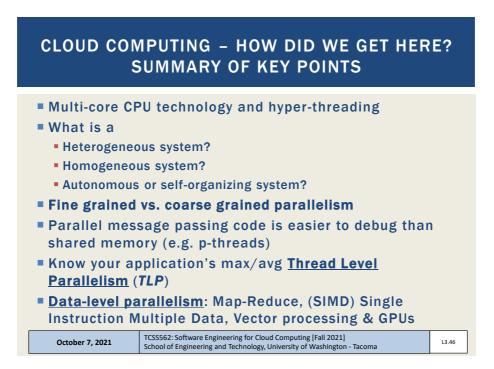










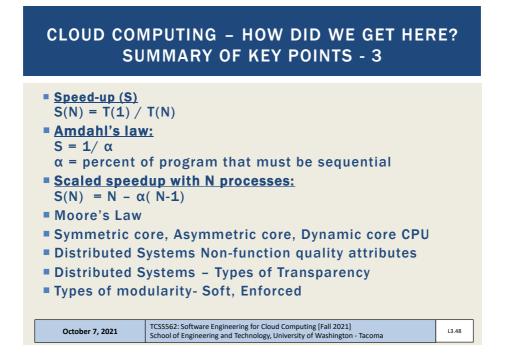


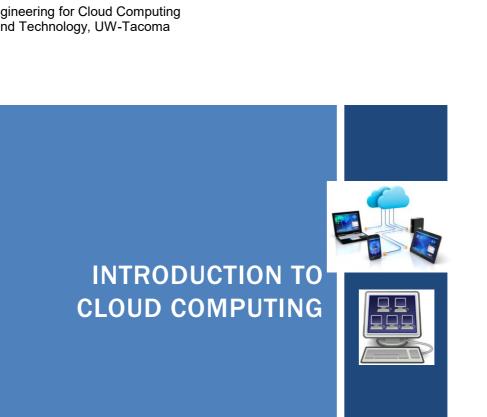
CLOUD COMPUTING – HOW DID WE GET HERE? SUMMARY OF KEY POINTS - 2



- Instruction-level parallelism (CPU pipelining)
- Flynn's taxonomy: computer system architecture classification
 - SISD Single Instruction, Single Data (modern core of a CPU)
 - SIMD Single Instruction, Multiple Data (Data parallelism)
 - MIMD Multiple Instruction, Multiple Data
 - MISD is RARE; application for fault tolerance...
- Arithmetic intensity: ratio of calculations vs memory RW
- Roofline model: Memory bottleneck with low arithmetic intensity
- **GPUs**: ideal for programs with high arithmetic intensity
 - SIMD and Vector processing supported by many large registers

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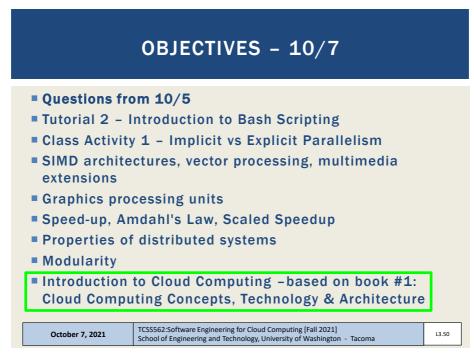


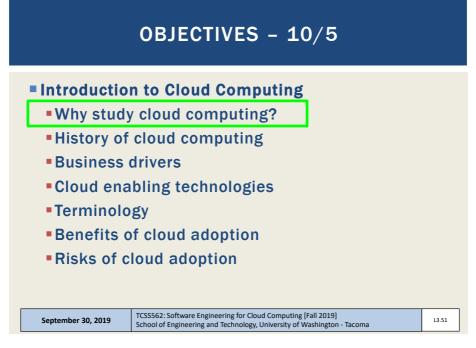
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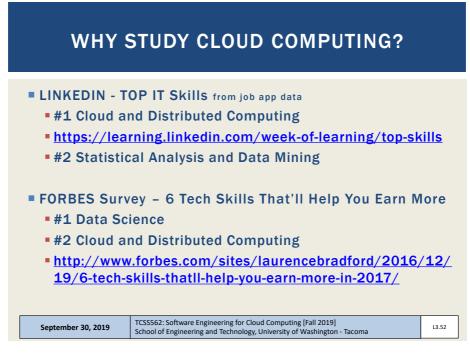
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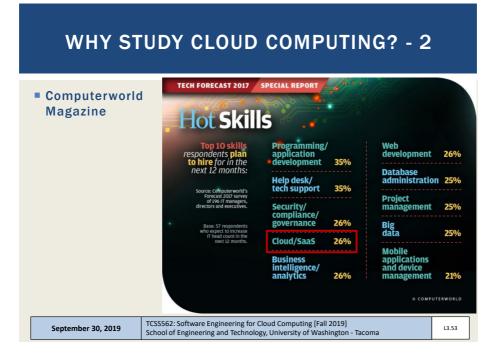


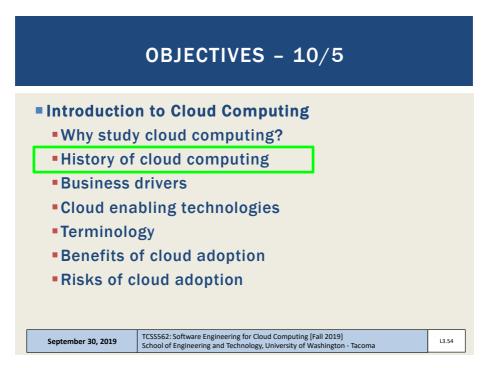
September 30, 2019

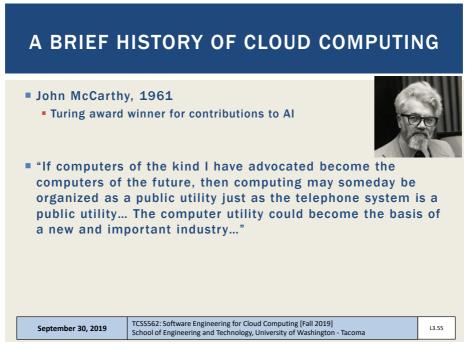


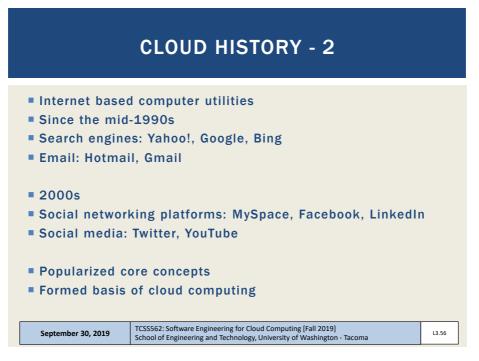


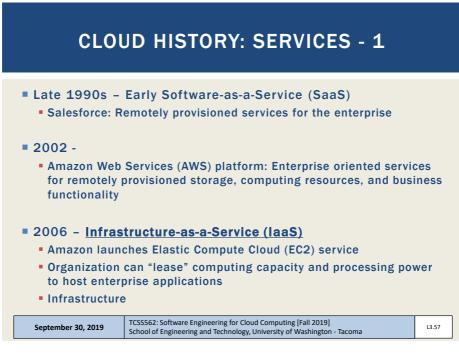










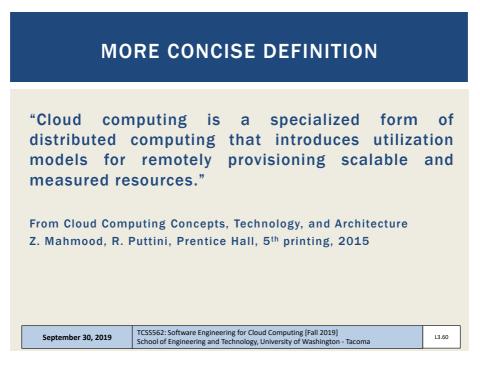


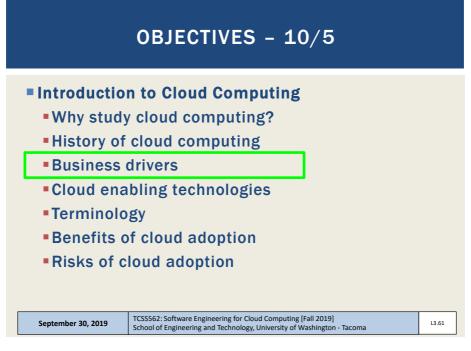


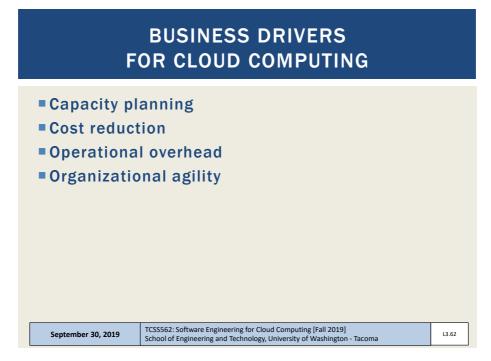


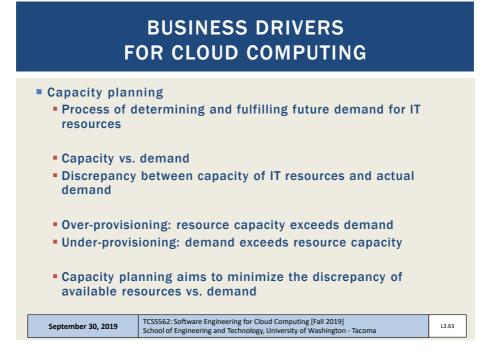
"Cloud computing is a model for enabling convenient, on-demand network access to a shared pool of configurable computing resources (networks, servers, storage, applications and services) that can be rapidly provisioned and reused with minimal management effort or service provider interaction"...



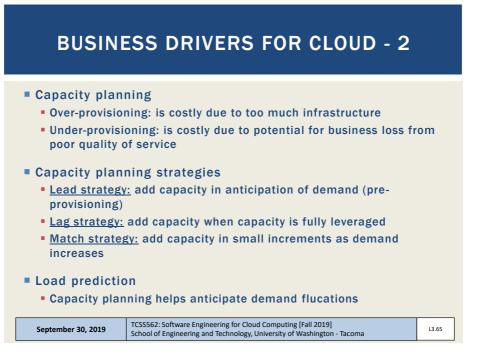


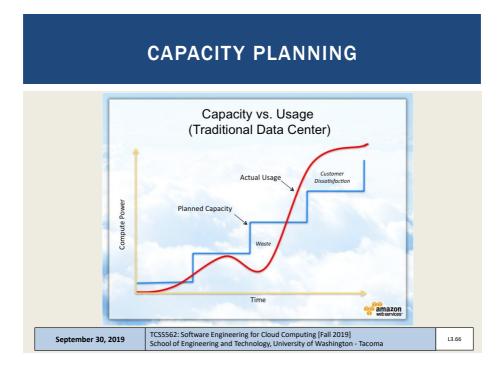


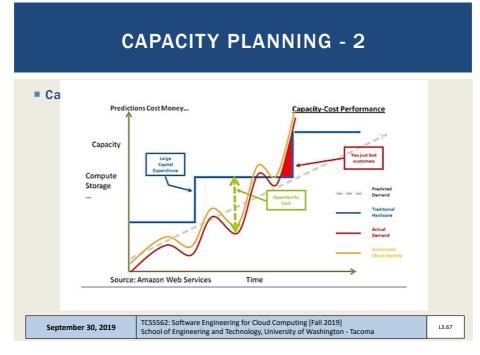


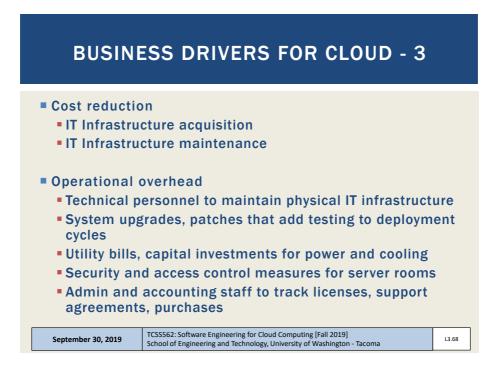


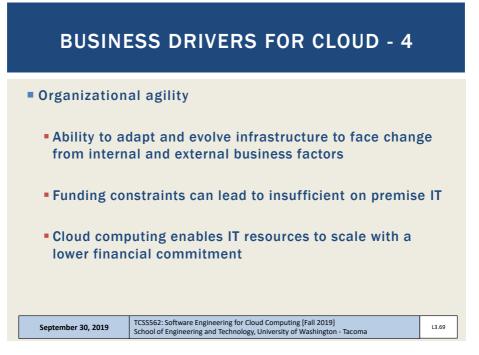


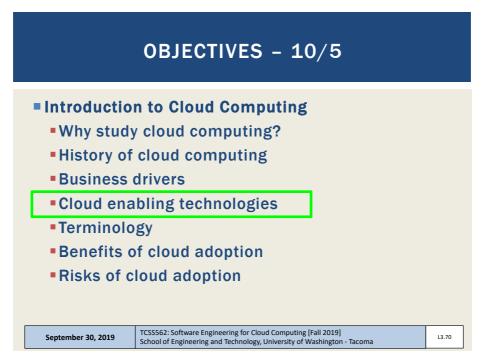


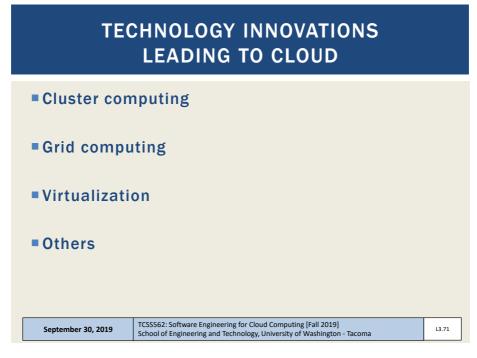


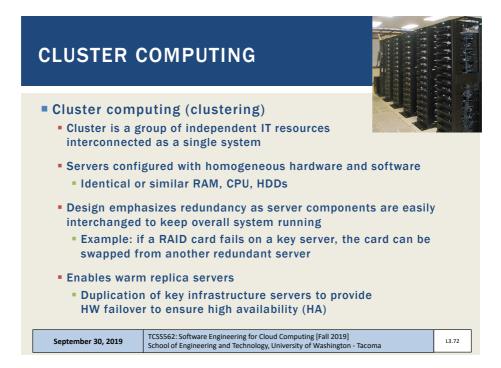


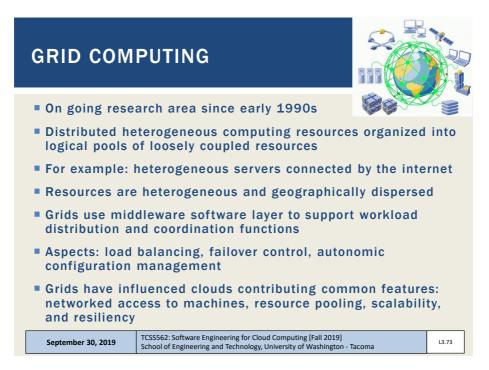


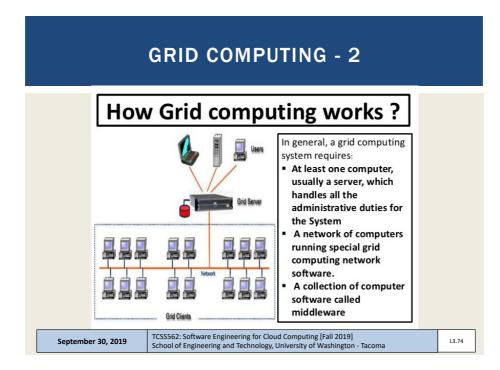






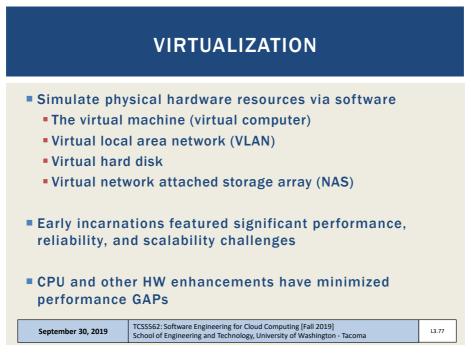


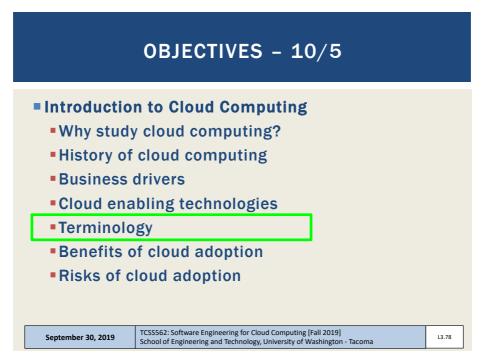


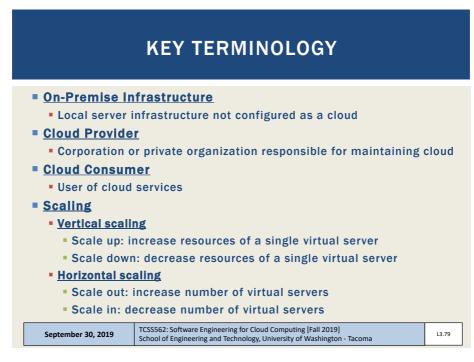


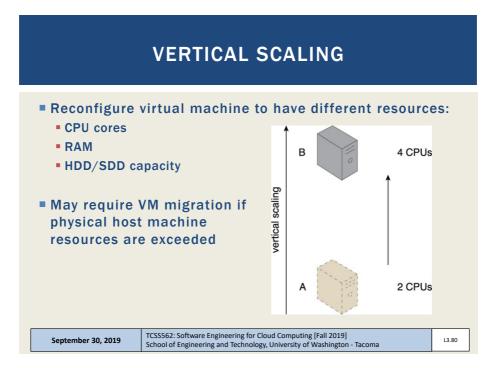
	VIRTUALIZATION	
	Virtual Machine OS Kernel Processes Drivers Hypervisor Hardware	
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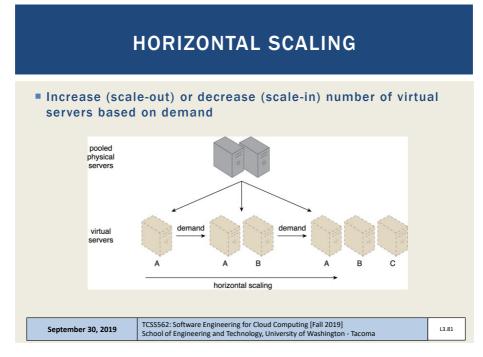
VIRTUALIZATION				
Virtual Machine	Virtual Machine	Virtual Machine	Virtual Machine	
OS Kernel	OS Kernel	OS Kernel	OS Kernel	
Processes	Processes	Processes	Processes	
Drivers	Drivers	Drivers	Drivers	
Hypervisor Hardware				
September 30, 2019	TCSS562: Software Engineering fo School of Engineering and Techno		Tacoma L3	



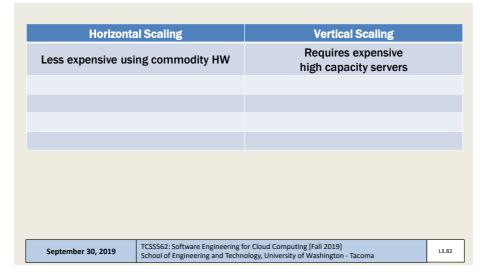








HORIZONTAL VS VERTICAL SCALING



HORIZONTAL VS VERTICAL SCALING

Horizontal Scaling		Vertical Scaling	
Less expensive using comm	odity HW	Requires expensive high capacity servers	
IT resources instantly ava	ailable	IT resources typically instantly availab	
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HORIZONTAL VS VERTICAL SCALING

Horizonta	al Scaling	Vertical Scaling	
Less expensive usi	ng commodity HW	Requires expensive high capacity servers	
IT resources ins	tantly available	IT resources typically instantly avai	ilable
Resource and automa	replication ated scaling	Additional setup is normally needed	
September 30, 2019	September 30, 2019 TCSS562: Software Engineering for Cloud Computing [Fall 2019] School of Engineering and Technology, University of Washington - Tacoma		

HORIZONTAL VS VERTICAL SCALING

Horizonta	l Scaling	Vertical Scaling	
Less expensive usi	ng commodity HW	Requires expensive high capacity servers	
IT resources inst	tantly available	IT resources typically instantly available	
Resource r and automa	•	Additional setup is normally needed	
Additional servers required		No additional servers required	
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HORIZONTAL VS VERTICAL SCALING

Horizontal Scaling	Vertical Scaling
Less expensive using commodity HW	Requires expensive high capacity servers
IT resources instantly available	IT resources typically instantly available
Resource replication and automated scaling	Additional setup is normally needed
Additional servers required	No additional servers required
Not limited by individual server capacity	Limited by individual server capacity

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