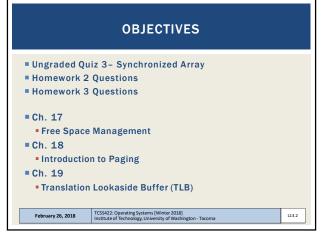
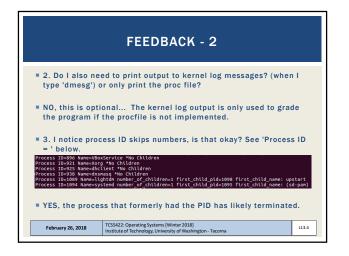


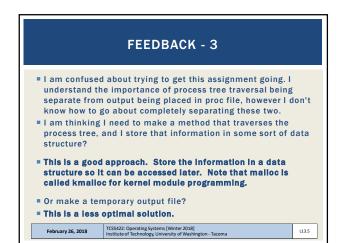
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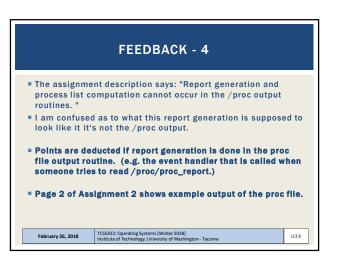
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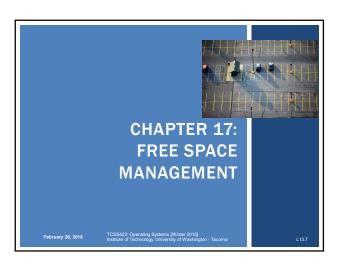


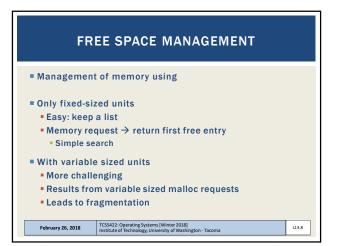


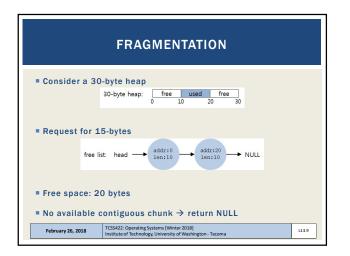


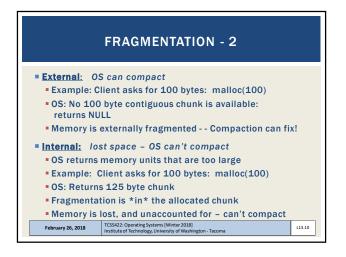


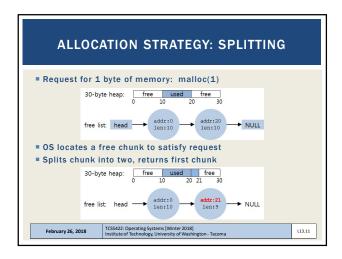


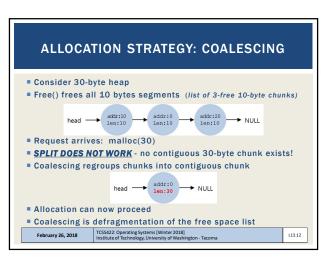


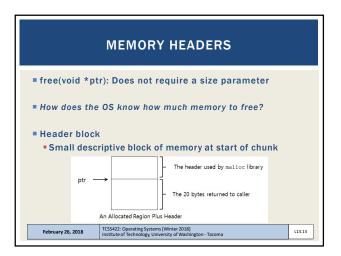


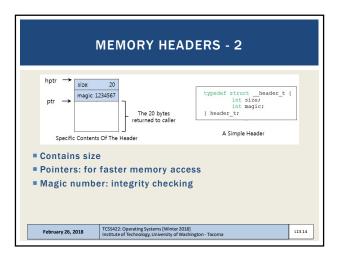


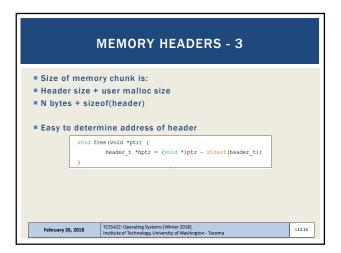




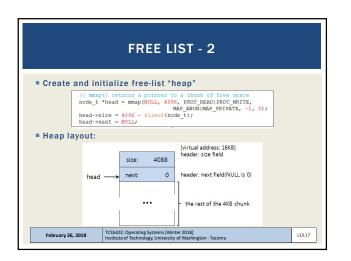


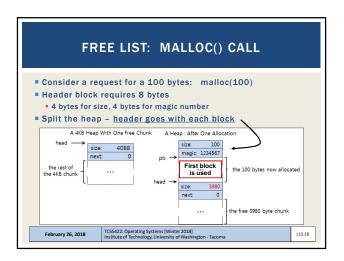


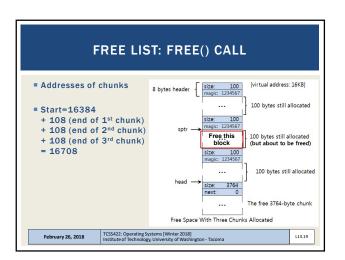


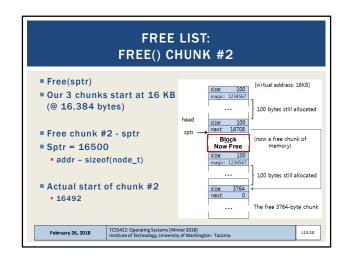


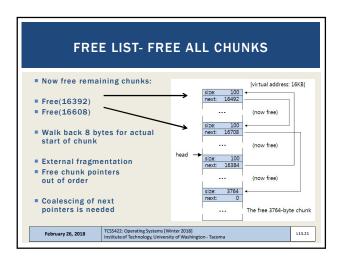


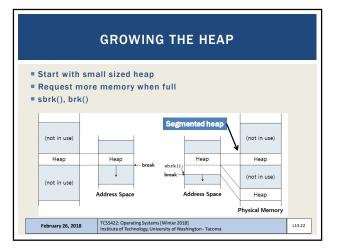


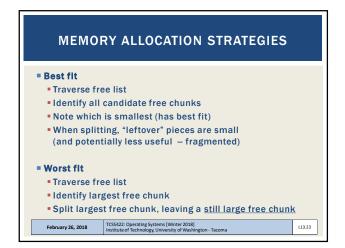


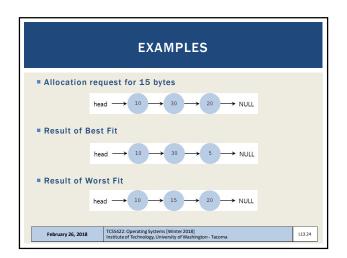






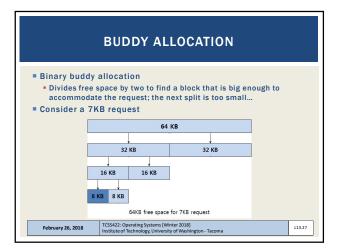


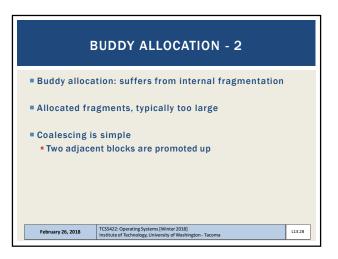


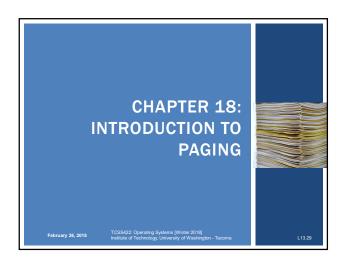


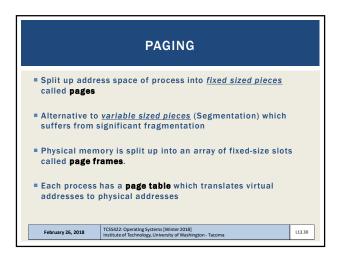


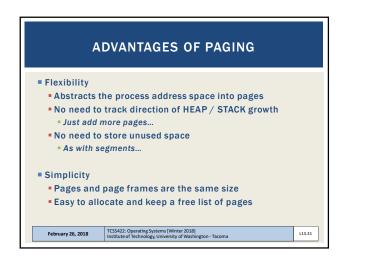


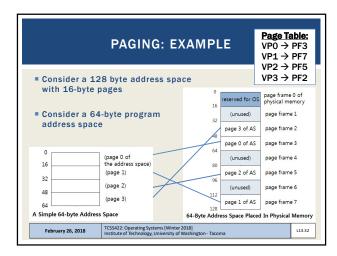


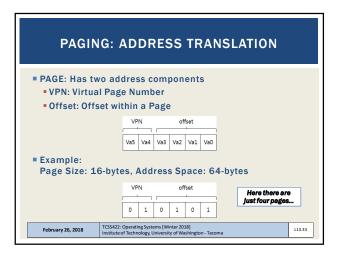


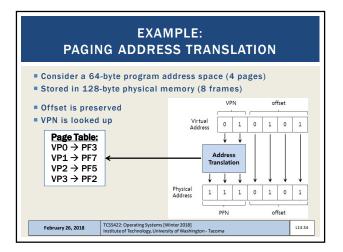


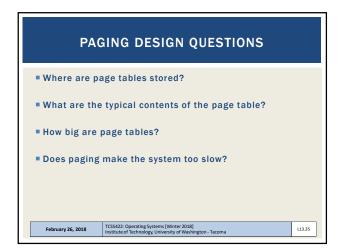


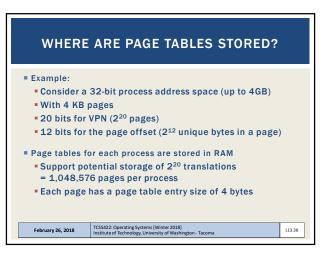


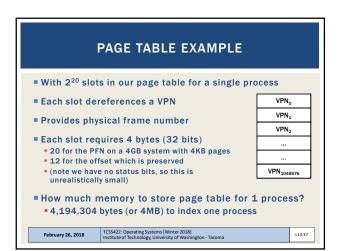


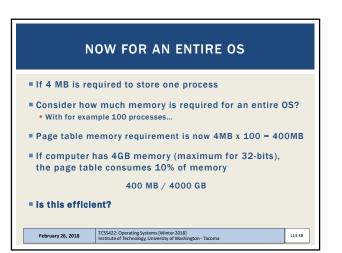


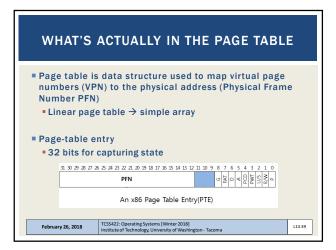


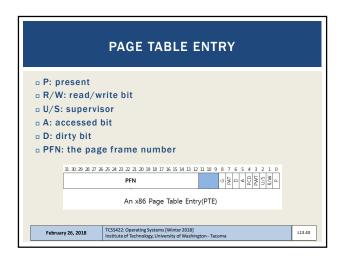


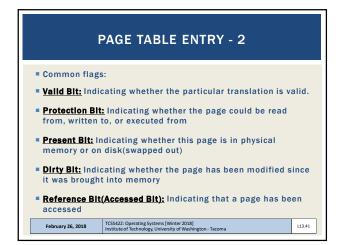


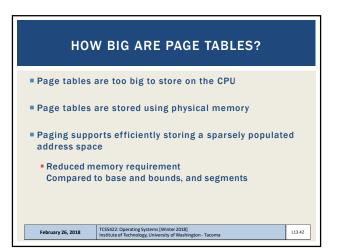












DOES PAGING MAKE THE SYSTEM TOO SLOW?			
Translation			
■ <u>Issue #1:</u> St needed	arting location of the page tab	le is	
 HW Support: Page-table base register stores active process 		Page Table: VP0 → PF3 VP1 → PF7	
Facilitate	es translation Stored in RAM →	$VP2 \rightarrow PF5$ $VP3 \rightarrow PF2$	
	ich memory address translation extra memory reference	n for paging	
HW Suppo	rt: TLBs (Chapter 19)		
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PAGING MEMORY ACCESS				
	ct the VPN from the virtual address irtualaddress & VPN_MASK) >> SHIFT			
4. // Form	the address of the page-table entry (PTE) = PTBR + (VPN * sizeof(PTE))			
7. // Fetch 8. PTE = Act 9.	the PTE cessMemory(PTEAddr)			
11. if (PTE.)	<pre>if process can access the page Valid == False) RaiseException(SEGMENTATION_FAULT)</pre>			
13. else if (CanAccess(PTE.ProtectSits) == False) 14. RaiseException(PROTECTION_FAULT) 15. else				
 // Access is OK: form physical address and fetch it offset = VirtualAddress & OFFSET_MASK PhysAddr = (PTE.PPN << PFN_SNIET) offset 				
19. February 26, 2018	Register = AccessMemory(PhysAddr) TCS5422: Operating Systems [Winter 2018] Institute of Technology, University of Washington - Tacoma	L13.44		

