



LOCKS - 2

- Lock variables are called "MUTEX"
 - Short for mutual exclusion (that's what they guarantee)
- Lock variables store the state of the lock
- States
 - Locked (acquired or held)
 - Unlocked (available or free)
- Only 1 thread can hold a lock

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L7b.5

LOCKS - 3

- pthread_mutex_lock(&lock)
 - Try to acquire lock
 - If lock is free, calling thread will acquire the lock
 - Thread with lock enters critical section
 - Thread "owns" the lock
- No other thread can acquire the lock before the owner releases it.

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LOCKS - 4

- Program can have many mutex (lock) variables to "serialize" many critical sections
- Locks are also used to protect data structures
 - Prevent multiple threads from changing the same data simultaneously
 - Programmer can make sections of code "granular"
 - Fine grained means just one grain of sand at a time through an hour glass
 - Similar to relational database transactions
 - DB transactions prevent multiple users from modifying a table, row, field

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FINE GRAINED?

Is this code a good example of "fine grained parallelism"?

```
pthread_mutex_lock(&lock);
a = b++;
b = a * c;
*d = a + b + c;
FILE * fp = fopen ("file.txt", "r");
fscanf(fp, "%s %s %s %d", str1, str2, str3, &e);
ListNode *node = mylist->head;
Int i=0
while (node) {
  node->title = str1;
  node->subheading = str2;
  node->desc = str3;
  node->end = *e;
  node = node->next;
  i++
e = e - i;
```

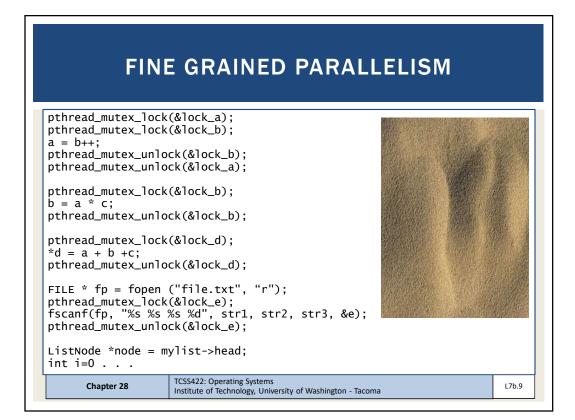


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pthread_mutex_unlock(&lock);

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EVALUATING LOCK IMPLEMENTATIONS

- Correctness
 - Does the lock work?
 - Are critical sections mutually exclusive? (atomic-as a unit?)



- Fairness
 - Do threads competing for a lock have a fair chance of acquiring it?
- Overhead

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BUILDING LOCKS

- Locks require hardware support
 - To minimize overhead, ensure fairness and correctness
 - Special "atomic-as a unit" instructions to support lock implementation
 - Atomic-as a unit exchange instruction
 - XCHG
 - Compare and exchange instruction
 - CMPXCHG
 - **CMPXCHG8B**
 - CMPXCHG16B

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HISTORICAL IMPLEMENTATION

- To implement mutual exclusion
 - Disable interrupts upon entering critical sections

```
1 void lock() {
2     DisableInterrupts();
3  }
4 void unlock() {
5     EnableInterrupts();
6 }
```

- Any thread could disable system-wide interrupt
 - What if lock is never released?
- On a multiprocessor processor each CPU has its own interrupts
 - Do we disable interrupts for all cores simultaneously?
- While interrupts are disabled, they could be lost
 - If not queued...

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SPIN LOCK IMPLEMENTATION

- Operate without atomic-as a unit assembly instructions
- "Do-it-yourself" Locks
- Is this lock implementation: Correct? Fair? Performant?



```
typedef struct __lock_t { int flag; } lock_t;
3
    void init(lock_t *mutex) {
         // 0 \rightarrow lock is available, 1 \rightarrow held
         mutex->flag = 0;
    }
   void lock(lock_t *mutex) {
8
9
        while (mutex->flag == 1) // TEST the flag
                 ; // spin-wait (do nothing)
         mutex->flag = 1; // now SET it !
11
12 }
13
14
   void unlock(lock_t *mutex) {
15
         mutex->flag = 0;
16
```

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DIY: CORRECT?

Correctness requires luck... (e.g. DIY lock is incorrect)

```
Thread1 Thread2

call lock()
while (flag == 1)
interrupt: switch to Thread 2

call lock()
while (flag == 1)
flag = 1;
interrupt: switch to Thread 1

flag = 1; // set flag to 1 (too!)
```

Here both threads have "acquired" the lock simultaneously

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DIY: PERFORMANT?

```
void lock(lock_t *mutex)
{
    while (mutex->flag == 1);
    mutex->flag = 1;
}
// while lock is unavailable, wait...
```

- What is wrong with while(<cond>); ?
- Spin-waiting wastes time actively waiting for another thread
- while (1); will "peg" a CPU core at 100%
 - Continuously loops, and evaluates mutex->flag value...
 - Generates heat...

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TEST-AND-SET INSTRUCTION

- C implementation: not atomic
 - Adds a simple check to basic spin lock
 - One a single core CPU system with preemptive scheduler:
 - Try this...

```
int TestAndSet(int *ptr, int new) {
    int old = *ptr; // fetch old value at ptr
    *ptr = new; // store 'new' into ptr
    return old; // return the old value
}
```

- lock() method checks that TestAndSet doesn't return 1
- Comparison is in the caller
- Single core systems are becoming scarce
- Try on a one-core VM

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DIY: TEST-AND-SET - 2

- Requires a preemptive scheduler on single CPU core system
- Lock is never released without a context switch
- 1-core VM: occasionally will deadlock, doesn't miscount

```
typedef struct __lock_t {
         int flag;
3
   } lock_t;
   void init(lock_t *lock) {
       // 0 indicates that lock is available,
// 1 that it is held
7
8
        lock -> flag = 0;
   }
10
11 void lock(lock_t *lock) {
       while (TestAndSet(&lock->flag, 1) == 1)
12
13
                ;
                         // spin-wait
14 }
15
16 void unlock(lock t *lock) {
17
        lock->flag = 0;
18
```

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SPIN LOCK EVALUATION

Correctness:

 Spin locks guarantee: critical sections won't be executed simultaneously by (2) threads

Fairness:

No fairness guarantee. Once a thread has a lock, nothing forces it to relinquish it...

Performance:

- Spin locks perform "busy waiting"
- Spin locks are best for short periods of waiting
- Performance is slow when multiple threads share a CPU
 - Especially for long periods

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COMPARE AND SWAP

- Checks that the lock variable has the expected value FIRST, before changing its value
 - If so, make assignment
 - Return value at location
- Adds a comparison to TestAndSet
- Useful for wait-free synchronization
 - Supports implementation of shared data structures which can be updated atomically (as a unit) using the HW support CompareAndSwap instruction
 - Shared data structure updates become "wait-free"
 - Upcoming in Chapter 32

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COMPARE AND SWAP Compare and Swap int CompareAndSwap(int *ptr, int expected, int new) { int actual = *ptr; if (actual == expected) 2 3 *ptr = new; return actual; 1-core VM: Spin loc Count is correct, no deadlock ; // spin X86 provides "cmpxchg1" compare-and-exchange instruction cmpxchg8b cmpxchg16b TCSS422: Operating Systems Chapter 28 L7b.20 Institute of Technology, University of Washington - Tacoma

TWO MORE "LOCK BUILDING" CPU INSTRUCTIONS

- Cooperative instructions used together to support synchronization on RISC systems
- No support on x86 processors
 - Supported by RISC: Alpha, PowerPC, ARM
- Load-linked (LL)
 - Loads value into register
 - Same as typical load
 - Used as a mechanism to track competition
- Store-conditional (SC)
 - Performs "mutually exclusive" store
 - Allows only one thread to store value

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LL/SC LOCK

```
int LoadLinked(int *ptr) {
   return *ptr;
}

int StoreConditional(int *ptr, int value) {
   if (no one has updated *ptr since the LoadLinked to this address) {
        *ptr = value;
        return 1; // success!
} else {
        return 0; // failed to update
}
```

- LL instruction loads pointer value (ptr)
- SC only stores if the load link pointer has not changed
- Requires HW support
 - C code is psuedo code

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