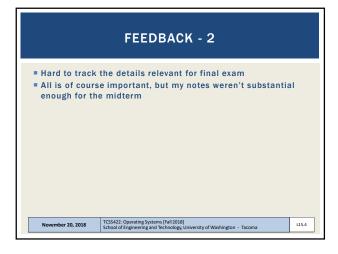
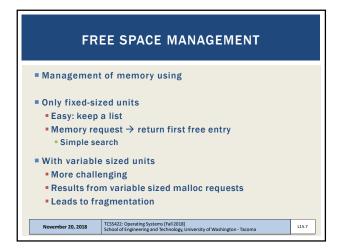


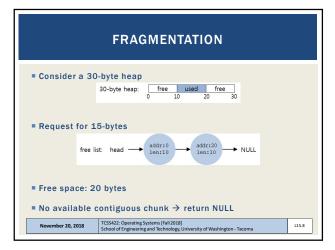
BRK(), SBRK()		
The "break", t sbrk(), is the of In traditional data segment Before the pro- the "text" and address zero a end of the dat The first call t up and create	low.com/questions/6988487/what-does-the-brk-system he address manipulated by brk() and dotted line at the top of the heap Unix (before shared libraries) the was continuous with the heap. gram starts, the kernel would load "data" blocks into RAM starting at and set the break address to the	heap data text
diagram, and subsequent use of malloc() would use it to make the heap bigger as necessary. November 20, 2018 TCSS422: Operating System [sill 2018] School of Endineering and Technology. University of Washington - Tacoma 115.3		



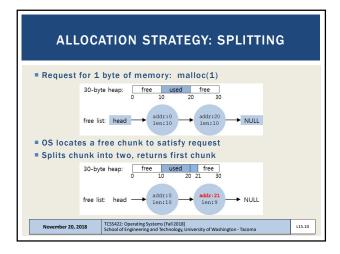
OBJECTIVES		
Quiz 4Program 2Program 3		
 Segments Chapter 17 - Free Space Management 		
 Paging Chapter 18 – Introduction to Paging Chapter 19 – Translation Lookaside Buffer 		
■ Chapter 20 - Paging Smaller Tables ■ Chapter 21/22 - Beyond Physical Memory		
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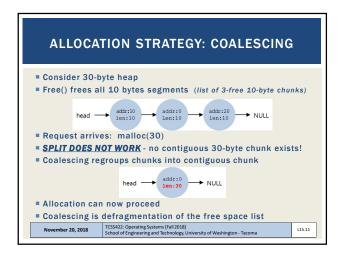


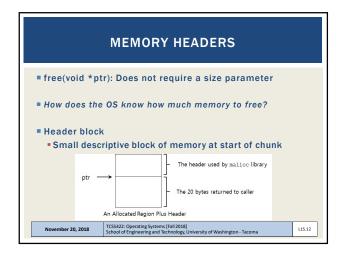


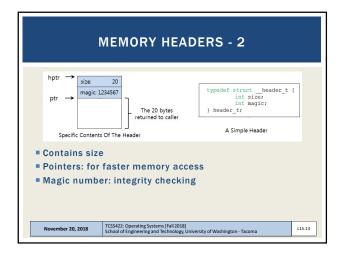


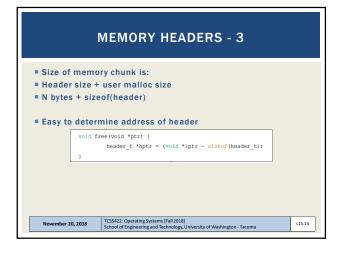
FRAGMENTATION - 2		
External: OS can compact		
Example: Client asks for 100 bytes: malloc(100)		
 OS: No 100 byte contiguous chunk is available: returns NULL 		
• Memory is externally fragmented Compaction can fix!		
Internal: lost space - OS can't compact		
OS returns memory units that are too large		
Example: Client asks for 100 bytes: malloc(100)		
OS: Returns 125 byte chunk		
 Fragmentation is *in* the allocated chunk 		
• Memory is lost, and unaccounted for – can't compact		
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```
THE FREE LIST

Simple free list struct

typedef struct __node_t {
    int size;
    struct __node_t *next;
} nodet_t;

Use mmap to create free list

4kb heap, 4 byte header, one contiguous free chunk

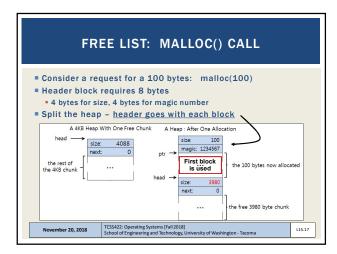
// mmap() returns a pointer to a chunk of free space
    node_t *head = mmap(NULL, 4096, PROT_READ)PROT_WRITE,
    head->size = 4096 - sizeof(node_t);

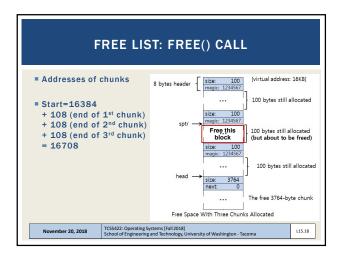
head->next = NULL;

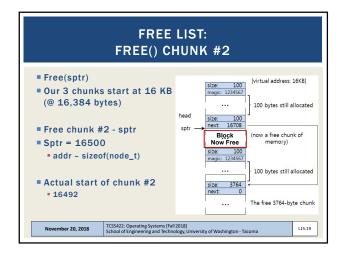
November 20, 2018

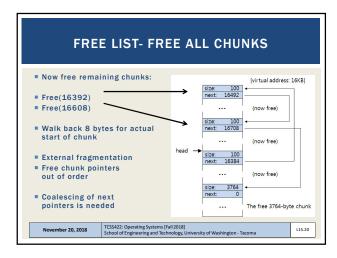
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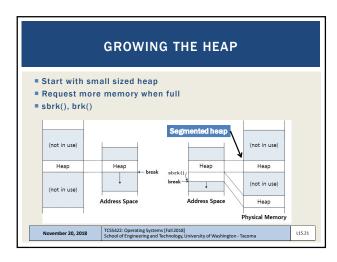


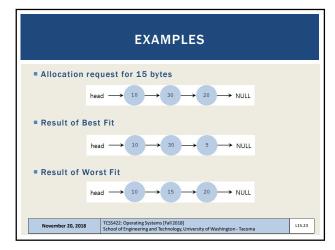




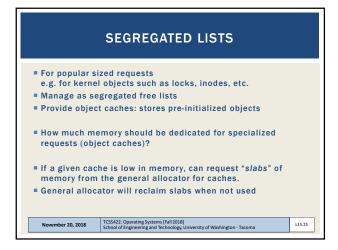


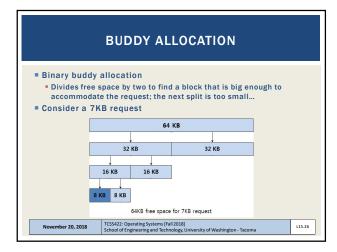




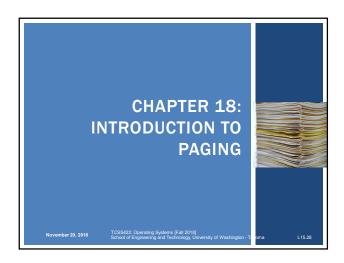


MEMORY	ALLOCATION STRATEGIES - :	2
• Find first chu	at beginning of free list nk large enough for request eturning a "fit" chunk, saving the remainder	
■ Next flt	e list traversal of best and worst fit	
Maintain a poHelps balance	inter that "cycles" through the list e chunk distribution vs. first fit nk, that is large enough for the request, and split	
Avoids full fre		
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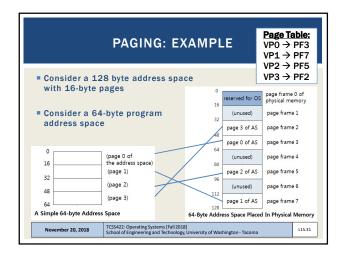


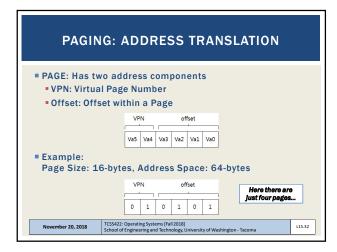
BUDDY ALLOCATION - 2 Buddy allocation: suffers from internal fragmentation Allocated fragments, typically too large Coalescing is simple Two adjacent blocks are promoted up TCSS42: Operating Systems [Fail 2018] School of Engineering and Technology, University of Washington-Tacoma

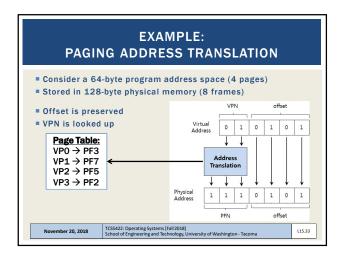


PAGING Split up address space of process into fixed sized pieces called pages Alternative to variable sized pieces (Segmentation) which suffers from significant fragmentation Physical memory is split up into an array of fixed-size slots called page frames. Each process has a page table which translates virtual addresses to physical addresses TCSS422: Operating Systems [Fall 2018] School of Engineering and Technology, University of Washington-Tacoma 115.29

ADVANTAGES OF PAGING Flexibility Abstracts the process address space into pages No need to track direction of HEAP / STACK growth Just add more pages... No need to store unused space As with segments... Simplicity Pages and page frames are the same size Easy to allocate and keep a free list of pages November 20, 2018 TCSS422-Operating Systems [fail 2018] School of Engineering and Technology, University of Washington-Tacoma



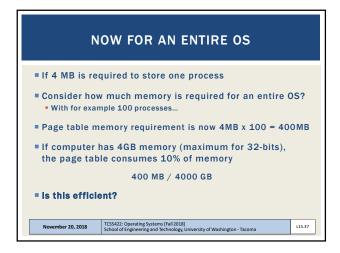




PAGING DESIGN QUESTIONS 1 (1) Where are page tables stored? 1 (2) What are the typical contents of the page table? 1 (3) How big are page tables? 1 (4) Does paging make the system too slow? 1 (4) Does paging make the system too slow?

(1) WHER	E ARE PAGE TABLES STORED	?
With 4 KB p20 bits for V	32-bit process address space (up to 4GB) pages /PN (2 ²⁰ pages) he page offset (2 ¹² unique bytes in a page))
Support pot = 1,048,576	r each process are stored in RAM ential storage of 2 ²⁰ translations 6 pages per process nas a page table entry size of 4 bytes	
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ı	PAGE TABLE EXAMPLE	
■ With 2 ²⁰ slot	s in our page table for a single proces	ss
■ Each slot dereferences a VPN VPN₀		VPN ₀
 Provides physical frame number Each slot requires 4 bytes (32 bits) 20 for the PFN on a 4GB system with 4KB pages 12 for the offset which is preserved 		VPN ₁
		VPN ₂
• (note we have no status bits, so this is unrealistically small)		PN ₁₀₄₈₅₇₆
	nemory to store page table for 1 pr bytes (or 4MB) to index one process	ocess?
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(2) WHAT'	S ACTUALLY IN THE PAGE TAB	LE
numbers (VP Number PFN • Linear pag	e table → simple array	e
31 30 29 28 27 2	86 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 PFN	
An x86 Page Table Entry(PTE)		
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PAGE TABLE ENTRY		
 P: present R/W: read/write bit U/S: supervisor A: accessed bit D: dirty bit PFN: the page frame number 		
31 30 29 28 77 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 PFN U S Q Q D S S S S S S S S S		
An x86 Page Table Entry(PTE) November 20, 2018 TCSS422: Operating Systems [Fall 2018] 115.39		

PAGE TABLE ENTRY - 2 Common flags: Yalld Bit: Indicating whether the particular translation is valid. Protection Bit: Indicating whether the page could be read from, written to, or executed from Present Bit: Indicating whether this page is in physical memory or on disk(swapped out) Dirty Bit: Indicating whether the page has been modified since it was brought into memory Reference Bit(Accessed Bit): Indicating that a page has been accessed November 20, 2018 TCSS42: Operating Systems [Fall 2018] School of Engineering and Technology, University of Washington-Tacoma

(3) HOW BIG ARE PAGE TABLES? Page tables are too big to store on the CPU Page tables are stored using physical memory Paging supports efficiently storing a sparsely populated address space Reduced memory requirement Compared to base and bounds, and segments **TCSS422:Operating Systems [Fail 2018] School of Engineering and Technology, University of Washington-Tacoma** L15.41

(4) DOES PAGING MAKE THE SYSTEM TOO SLOW?		
■ Translation		
Issue #1: Starting location of the page table is needed		
 HW Support: Page-table base register stores active process Page Table: VPO → PF3		
■ Facilitates translation Stored in RAM → VP1 → PF7 VP2 → PF5 VP3 → PF2		
• Issue #2: Each memory address translation for paging requires an extra memory reference		
HW Support: TLBs (Chapter 19)		
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