TCSS 422: Operating Systems Fall 2016

Institute of Technology University of Washington – Tacoma

Practice Quiz 3 – Memory Management

Wednesday November 23rd, 2016

Question 1 – Base and Bounds

A computer system uses a simple base/bounds register pair to virtualize address spaces. In each of the traces below, your job is to fill in the missing values of virtual addresses, physical addresses, base, and/or bounds registers. In some cases, it is not possible to provide an exact value. If so, please specify a range (e.g. greater than 100), or value that is not a single number.

Virtual Address \rightarrow	Physical Address			
100	800			
300	1000		Base?	
799	1499			
800	[fault]		Bounds?	
Virtual Address $ ightarrow$	Physical Address			
400	2500		Base?	
1700	3800			
2001		?	Bounds?	
3001	5101			
Virtual Address $ ightarrow$	Physical Address			
	_ 1400		Base?	500
	_ 2200			
	_ 2499		Bounds?	2000
	[fault]			

Question 2 – Page Tables

Compute memory requirement for each of the following page table implementations.

Consider a computer with 64KB of physical memory, where the page size is 256 bytes.

For a single-level page table, how many pages are there?

How many bits are required for the virtual page number (VPN)?

How many bits are required for the offset, considering that we would like the ability to address any byte in a 256 byte page?

What is the total space requirement in bytes for this single level page table?

Now consider a two level page table. At the first level we have a page directory which divides the page space in half. Half of the VPN bits are used to index the page directory, while the other half support indexing a page table. The page directory provides references to page tables which refer to pages.

If we create and store 4 pages indexed by a page table in the second level, what is the total space requirement in bytes for this two-level page table?

Question 3 – TLB Hit/Miss Ratio with LRU

Consider a TLB with a 5-address capacity which utilizes the Last Recently Used (LRU) cache replacement policy. Given the following page requests, what is the ratio of cache hits to misses?

The 5-address TLB has the following initial state sorted newest to oldest:

TLBO	7
TLB1	9
TLB2	3
TLB3	5
TLB4	1

Cache arrival sequence:									
0	3	5	2	1	7	8	2	3	4

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Misses:

Ratio: ______