Silicon Wafer Engineering and Defect Science Center (SiWEDS)

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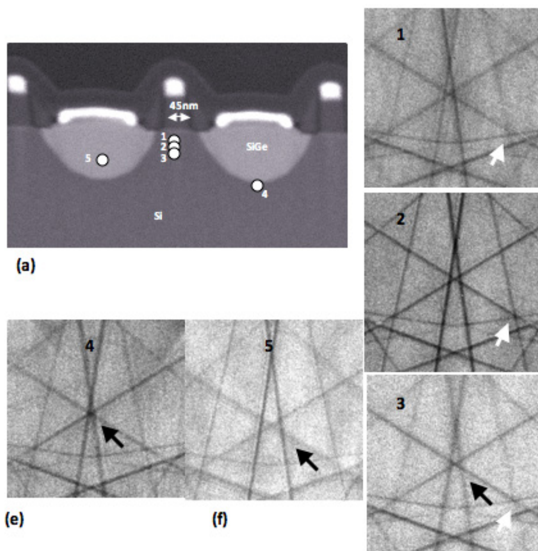
Convergent Electron Beam Diffraction (CBED)



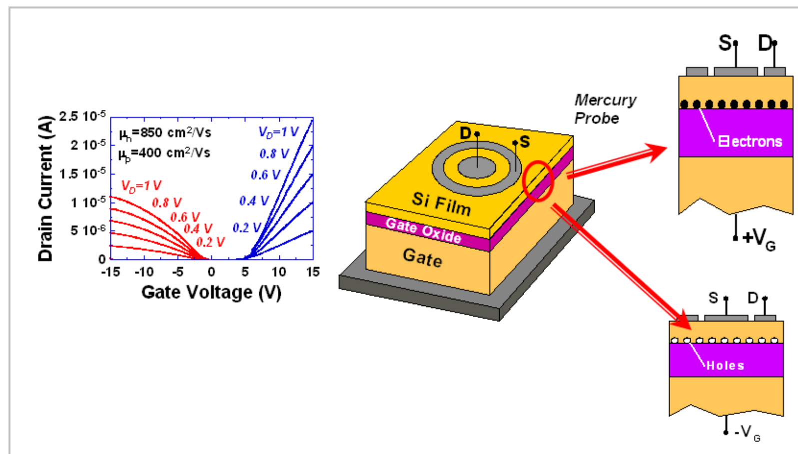
Control of a number of transistor properties, such as enhanced mobility through either substrates with stressed surface layers or process induced stressed channels, present long standing and difficult challenges. With device size decreasing, local strain variation on a nanoscale level is critical for device performance. Convergent electron beam diffraction (CBED) can provide strain information with a nanoscale spatial resolution and precision. Characterization of local strain information with CBED also can be a challenge due to HOLZ lines splitting and broadening. Researchers at the Center for Silicon Wafer Engineering and Defect Science (SiWEDS) representing three different universities have developed improved quantitative analysis of this HOLZ line splitting and residual strain measurements. Popular strain measurement techniques like Raman spectroscopy and X-ray diffractometry cannot satisfy current requirements for spatial resolution and precision as well as CBED technique does. HOLZ line splitting profile with CBED is a fast evaluation tool for initial strain state on different strain enhanced heterostructures.The experimental data and simulation results match well. This advance represents an important new method for reliable determination of strain in device structures with combinations of residual strain and elastic deformation. For example, improved direct measurement of stress in nanosized, buried areas such as the stressed channel have been demonstrated. For more information, contact G. Rozgonyi, North Carolina State University, 919.515.2934, rozgonyi@ncsu.edu, Eicke Weber, the University of

California, Berkeley, 510.642.0205, weber@socrates.berkeley.edu or Moon Kim at the University of Texas-Dallas, 972.883.6635, moonkim@utdallas.edu.

Previous image: Frame (a) is a Z-contrast TEM image which shows the structure of a 65nm PMOS node with a 45nm long gate and embedded SiGe at source and drain. The numbered white spots show the positions that the clean CBED patterns were taken from. The corresponding CBED patterns are shown in (b)-(f) with the white and black arrows indicating the HOLZ line shifts which enable a nanoscale strain profile to be calculated across the device.

Nondestructive Characterization of Silicon-on-Insulator Wafers

Silicon-on-insulator (SOI) is a preferred technology for leading edge, small devices in future integrated circuits. However, one of the challenges is the measurement of the thin silicon layers that make up the active portions of the circuit. Such measurements should be simple and be nondestructive so that wafers can be measured upon receipt. Arizona State University, a participant in SiWEDS Center research, has developed in conjunction with Four Dimensions, Inc., the manufacturer of the mercury probe, a technique using this probe to serve as source and drain of the MOSFET. Measurement of the thin silicon layers are now simple and non-destructive so wafers can be measured upon receipt. The device allows the current to be measured from which one extracts the carrier mobility, a very important device parameter, the threshold voltage, defect information, and the doping concentration. The technique is used by some of the SOI wafer producers, e.g., Gritek, MEMC, Komatsu, and LG Siltron. For more information, contact Dieter K. Schroder, Arizona State University, 480.965.6621, schroder@asu.edu.



Right: Schematic of *Hg* probe pseudo MOSFET and typical I_D-V_G curves. Both *n*-channel and *p*-channel parameters can be characterized.

Comprehensive model of properties of copper in silicon

The copper interconnect technology has become the mainstream technology for the manufacturing of high performance chips. This requires development of procedures and tools for contamination control of copper in silicon wafers and for removal of Cu from reclaim wafers. University of California at Berkeley, a participant of the SiWEDS Center, studies diffusion, electrical properties, and gettering of copper in bulk silicon. In the framework of this research, several breakthroughs were achieved in the area of understanding the fundamental physical properties of copper in silicon. It was demonstrated that the diffusion barrier for copper is silicon is not 0.43 eV, as it was thought for nearly forty years, but only 0.18 eV. Correspondingly, the diffusivity of Cu at room temperature is about three orders of magnitude higher than it was thought. This allows copper to diffuse substantial distances in silicon at room temperature and explains the kinetics of the phenomena of Cu contamination during chemomechanical polishing and of its outdiffusion to the surface during storage at room temperature. This data was provided to SiWEDS member companies, which used it for improving their technological processes. The ongoing collaborative effort between Intel and several wafer suppliers to develop a standard metrology of Cu contamination control relies to a large extent on this data. For additional information, contact Andrei Istratov, 510.486.6634, istratov@socrates.berkeley.edu or Eicke Weber, 510.642.0205, weber@socrates.berkeley.edu.

Process of Interfaceless Oxynitride Thin Layer

Dr. A. Karoui and Prof. Rozgonyi's team at the NC State University have developed methods for growing shallow oxynitride layers with unique properties on silicon wafers. The starting material is nitrogen doped commercial Czochralski Si, with an initial nitrogen level of about 1E15 cm^{-3}, lower levels can be used for growing shallower layers. The strong N segregation enriches the subsurface zone, which results in oxygen gettering. Unlike deposited oxynitride layers, the new layers are grown from the bulk with a smooth N and O concentration gradients. At a few microns away (or less) from the surface, N and O concentrations are increasing and peaking at the surface. The interfaceless oxynitride thing layers grown with this method are crystalline, continuous and interfaceless thus do not have interface states, known to be harmful for charge carriers. In addition, no charge center exists in these crystalline oxynitride unlike the amorphous ones grown by chemical vapor deposition. Knowing that interface states and charged centers found in add on oxynitride layers can be detrimental for devices, the new oxynitride layer are of interest for IC technology. Depending on the layer thickness and the [N] to [O] ratio, three novel processes are used: 1) Fine sliced N doped Si wafers are grinded to generate submicrometer roughness while exerting mechanical stress on the surface, then finely polished by chemical and mechanical polishing process (CMP). The thickness of the layer is in the nanoscale range, up to 0.5 microns. The nitrogen concentration reaches eight times and oxygen twice their respective solubility limits. 2) Anneal N doped wafers at 650°C for 8 hours, then at 1050°C for 10 hours. This process results in N and O concentrations up to 1E18 cm^{-3} and 2E20 cm^{-3}, respectively. The maximum breadth of this layer is 1.5 microns. 3) Anneal at 650°C for 16 hours, NCZ silicon wafer. For N doping level of 5E14 cm^{-3}, this process gives the maximum layer breadth, about 2 microns. For more information, contact Abdennaceur Karoui, NCSU, 919.515.7217, nas_karoui@ncsu.edu.