Center for Embedded Systems (CES)

A CISE-funded Center

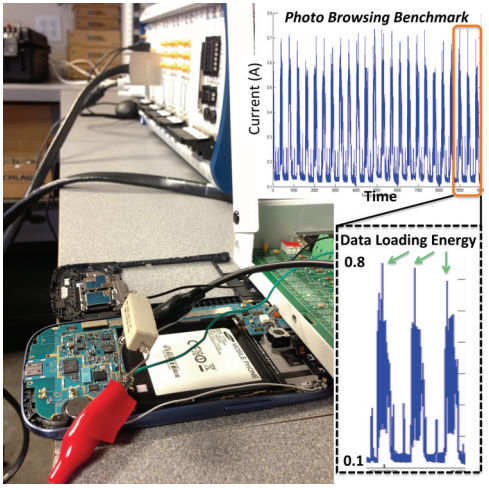
Arizona State University, Sarma Vrudhula, Director, 480.727.4152, vrudhula@asu.edu

Southern Illinois University – Carbondale, Spyros Tragoudas, 618.453.7027, spyros@engr.siu.edu

Center website: http://www.ces.asu.edu

Optimizing Energy Efficient Mobile Computing: Explicit Data Communication and Power Management Tool

For manufacturers of microelectronic systems such as smart phones, tablets, and other mobile computing devices and for SoC (system-on-a-chip) designers, manufacturers, and vendors, system power consumption represents a major consideration. SoC designers must optimize power within SoC units, such as CPUs, graphic controllers, display controllers and memory controllers. However, on modern mobile platforms most energy is consumed by data moving between CPUs and memory and display controllers. Researchers at Arizona State University's Center for Embedded Systems (CES) have been working to make SoC architecture and systems more power efficient. This breakthrough work led to the development of a tool that better analyzes power consumption of mobile applications within each unit so as to optimize SoC power efficiency by separating data movement and computation power.



Mobile platform energy consumption is measured using the National Instrument Energy Measurement and Data Collection Equipment. With the availability of the MobileBench workloads, CES researchers are a step closer to quantifying the increasing amount of data movement energy for modern smart phone architectures. This new CES-developed data communication and power management tool represents an improvement over previous state of the art because it is open source software instrumentation that SoC and other companies can use.

MobileBench is a mobile platform benchmark suite that runs on the Google Android's operating system. MobileBench contains a suite of commonly used smart phone applications that model interactive user behaviors to extract real-world energy usages for mobile platforms. SoC designers are beginning to use the tool for more effective assessments of power consumption. This work is helping the electronics industry produce more efficient SoCs for use in devices that will require less power support. Furthermore, with the insights provided by MobileBench into smart phone application characteristics, the ASU researchers hope to influence the design of future smart phone platforms toward having simpler architectures that lead to lower power consumption and higher performance.

Economic Impact: This energy-efficient mobile platform research tool addresses some of the most critical problems facing society at large, namely, improving microelectronic system energy efficiency, which continues to proliferate at exponential rates. Successful outcomes of the MobileBench tools will result in IAB member companies licensing this CES technology. MobileBench's novel approach to energy consumption is beginning to be used by member companies (e.g., Marvell plans to use this work to better analyze current products for embedding into smart phones and tablets) to create more energy-efficient mobile computing platforms that provide longer lasting connectivity in urban, rural, and energy-challenged areas. This, in turn, should allow for a more ubiquitous computing paradigm. For example, arctic exploration teams could harness the computing power and sensors of mobile computing devices for data extraction, computation, and publishing without having to carry electric generators, thus saving significant energy and resources. The approach also can be applied to even lower-power devices that make up the internet-of-things. This will make it easier to study and optimize energy consumption and should help make computing platforms and devices more connected and unplugged for longer periods. The work has the potential for significant positive economic benefits to the nation and to the electronics industry beyond national boundaries. It may also have significant positive impacts on the environment. Such impacts are difficult to quantify economically. Even so, it is likely that more efficient and lower power processors and other SoC processing elements will have direct impacts on consumer electronics that rely on a billion kWh of electricity. This alone could generate savings of nearly a billion million metric tons of CO_2. Even if this project resulted in only a 5% reduction in energy consumption of the billions of such mobile platforms worldwide, that could reduce the amount of CO_2 released into the atmosphere by hundreds of millions of metric tons per year and annually realize ten of millions of dollars in energy cost savings.

For more information contact Carole-Jean Wu, 480.965.1494, carole-jean.wu@asu.edu.

Design Tool for Mobile Low-power Processors

Mobile low-processor chips have evolved from single core processors into multi-core architectures that integrate 10-20 processor cores, 40-60 customized hardware units or accelerators, and many memory blocks. In other words, the state-of-the-art mobile processors integrate upwards of a hundred fairly complex intellectual property (IP) blocks into a single chip.

There are incessant calls for higher performance, lower power requirements, and shorter times to market. The on-chip interconnection architectures that connect these IP blocks together in cohesive systems have emerged as a key determinant of mobile processor performance and power consumption. These interconnected architectures are implemented as a Network-on-Chip (NoC) that consists of interconnected routers and IP blocks.

Embedded smart devices such as cellular phones and tablets have emerged as the new technology drivers for the semiconductor industry.

CES researchers have developed a computer-aided design (CAD) tool chain for developing the NoC architecture for future Qualcomm mobile processor chips. The NoC tool chain automatically generates high performance, low power on-chip interconnection architectures that are able to successfully address multiple traffic classes, multiple use-cases, deadlock avoidance, multiple clock islands, and bit-width optimization. In minutes, the tool chain is automated and performs design task that can take several weeks of manual effort. Consequently, the synthesized interconnection architecture and the overall mobile processor depict better performance, lower power consumption, and less time to design. The next generation smart phone products will have much higher performance requirements with the same or incrementally longer battery life times. Consequently, future generations of mobile processor chips will integrate ever-increasing numbers of IP blocks on the same chip. The NoC design tool developed by the CES team is a key technology that will enable Qualcomm to maintain its dominant position in the mobile low power processor market.

> **Economic Impact:** A center sponsor, Qualcomm Inc., is the market leader in mobile low-power processors aimed at smart phones and tablets. There are an estimated 5.2 billion cellular phone subscribers worldwide. It is expected that the number of low power mobile processors that are utilized by such devices will hit the 500 million mark by 2015. The increases in efficiency and development savings can be expected to have substantial economic impacts on the electronics industry and on the nation's competitive position.

For more information, contact Karam Chatha, 480.727.7850, KChatha@asu.edu.

Safer In-Vehicle Control Systems and Medical Devices

Embedded computing devices are becoming ubiquitous in our modern societies. It has been estimated that in developed countries there are about 30 embedded computing devices per person. Such devices are mostly operating safety critical systems such as medical devices, flight control systems, communication systems, and safety control features in automobiles; high-end vehicles alone often contain upwards of 60 embedded processors.

Automotive, aerospace, and medical device systems are safety-critical. Design methodologies that can improve confidence in overall system design are highly sought after by industry. One such design methodology is the Model Based Development (MBD) framework where the design of the system starts with a model of the system. Such models are usually developed in a modeling environment that supports a block diagram Graphical User Interface (GUI). GUIs enable modeling of both the physical components of a control system (e.g., modeling of an automobile engine), as well as the cyber components (e.g., modeling the software that controls engine performance).

CES Researchers in collaboration with researchers from University of Colorado, Boulder, and engineers from Toyota have developed S-TALIRO. S-TALIRO is a software tool that systematically checks a given system's model by searching for an input that demonstrates that a functional requirement is not satisfied. Such a functional requirement could be that the engine never stalls while the vehicle is cruising. The process of discovering operating conditions that produce a system behavior that violates a functional requirement is referred to as falsification. Even when falsifying behaviors cannot be found, system behaviors that come "closest" to violating the correctness property are typically returned to system designers.

The advantage of this technology over previous approaches is its applicability to industrial systems. Most alternative verification methods seek a mathematical proof that a property is satisfied. Unfortunately, these mathematical methods do not scale to the complexity of typical industrial control applications, nor do they mathematically "understand" the model's semantics. Because S-TALIRO is a simulation-based approach, it is immune to these difficulties and, thus, is a more robust 'model-based verification' framework that for the first time is being made available to industry.

Modern medical devices, airplanes, and cars include embedded software that interacts with the physical environment. Errors in the software can have catastrophic impact both in human lives and in economic costs to the society. S-TALIRO can support testing and verification of embedded software.

Economic Impact: Embedded systems must remain operational and reliable for many years. Their software cannot be easily updated. Failures in such systems due to software programming or logic design errors can have catastrophic consequences to human lives and large economic costs to our societies as a whole. Model Based Development (MBD) practices can help eliminate implementation errors. More importantly they can discover design errors very early in the design process. There is a clear need for tools that verify the correctness of a system with respect to functional requirements early in the design process. S-TALIRO can support such verification activities at multiple stages of the MBD cycle. In 2009, the global embedded systems market was estimated to be $208 billion with a yearly growth rate of about 10%. The embedded software itself grows at a rate of 10-30% depending on the application area. Over a decade ago NIST estimated that the annual costs of inadequate infrastructure for testing general purpose software could be as high as $59.5 billion. It is within the realm of possibility that S-TALIRO could help reduce development costs by at from 5% to 37%.

For more information, contact Georgios Fainekos, 480.965.8267, fainekos@asu.edu.