Center for Electromagnetic Compatibility (CEMC)

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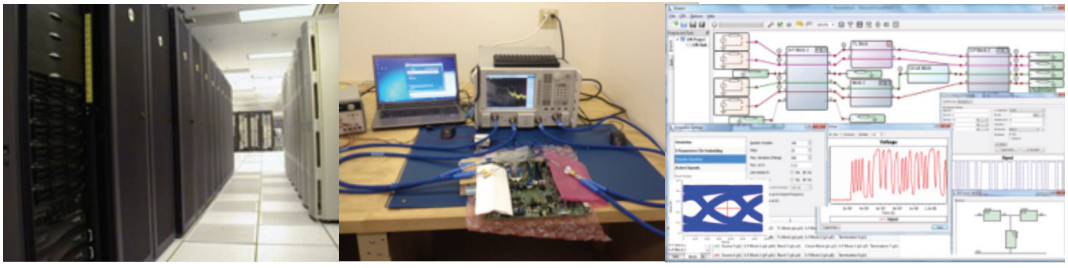
High Speed Link Path Analyzer: A Toolset for Decreasing Time to Market

Computer, Internet, and wireless communication generally are the revolutionary technologies that continue to significantly impact everyday life in our modern era. Every year new products are developed with new functionalities, improved performance, and easier user interfaces. The hardware designs required by these products are increasingly based on high-speed link-path analyses to ensure that the developed circuits operate properly with ever increasing speed, as well as diminishing size and power consumptions.

While high-speed link-path analysis is critical to achieve the normal operation of today's computer and electronic devices, the tools to simulate and model the geometries/components used in the link paths are often too basic and not easily consolidated. To analyze new products, engineers must use multiple tools from different vendors, a process that demands much time and deep knowledge and understanding of how the tools work. However, most designers of high-speed products often lack the resources to acquire the needed analytical tools or the time to become proficient at using them.



(Left) A massively parallel computing platform that uses high-speed links for data communication: an example end product that can benefit from the developed tool set; (Center) Laboratory measurement of a high-speed link: expensive instruments and expertise in high-frequency measurement are needed; (Right) A screenshot of the developed tool set for high-speed link-path analysis: cost-effective and no need for extensive training for the user.

To address the myriad of challenges faced by the high-speed design community, the Center for Electromagnetic Compatibility (CEMC) has developed a dedicated tool suite for high-speed link-path analysis. This innovative tool set not only consolidates most - if not all - of the tools needed to model and simulate high-speed designs, but it also provides holistic views of designs from die levels inside the chip to full system architectures. In addition, the tool set includes power integrity and power-distribution-network analysis,

enabling the co-simulation of signal and power integrity that is necessary when the products are operating at ever increasing speeds.

Within the unique partnership model of the I/UCRC, tool development was guided by the center's industry partners. As a result, the tool set fits well with "real-world" engineering practice. It can be easily integrated into the design process because it removes the need for users to understand the back-end theories, algorithms, and mathematics.

This work represents a significant improvement over the previous state of the art because it: 1) reduces the high costs involved with procuring multiple tools (often over $200K a year); 2) does not require extensive training of hardware designers; 3) can provide flexible signal and power integrity for co-simulations; 4) covers all aspects of the design from chip to system levels; and, 5) enables new features to be easily added. Recent research is enabling the tools to be more accurate and more capable of handling complex real-world problems more efficiently.

The software runs on multiple PC/workstation/server platforms and can import geometries from almost any design tool. A variety of features are available in the tool for users to perform, for example, eye diagram analysis, channel optimization, jitter decomposition, and other parameters and methodologies that are needed to validate advanced designs. Then, when results appear satisfactory, users can use the data to finalize and/or make necessary design modifications.

> **Economic Impact**: The developed tool set has been used in several CEMC member companies including Cisco, IBM, and Altera. In Cisco alone, use of the tools has already resulted in a cost reduction in commercial tool purchases in the amount of approximately $200K a year. When the tool set is further rolled out the total estimated cost reduction can reach as high as $2M a year. Because tool use does not require extensive training, Cisco has been realizing cost reductions of roughly $100K annually. Increased productivity of their engineers has been estimated to be approximately $300K. Lastly, time to market can be reduced because fewer prototypes are needed. We estimate related savings of about $300K per year for Cisco and up to $3M per year across all CEMC members. On the R&D side, having an integrated tool set helps evaluate new technologies needed for next generation products, which is extremely valuable for pre-development research.

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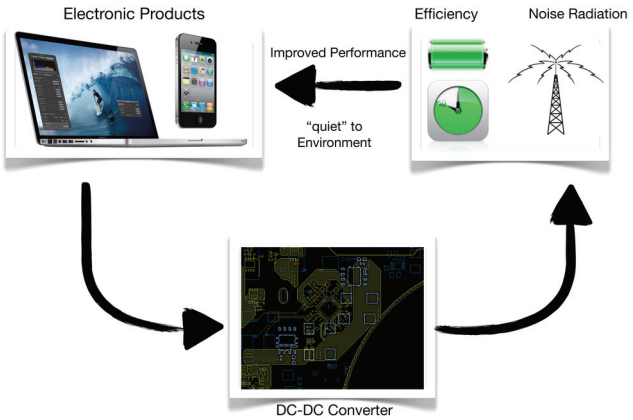
Reducing Emissions From DC-DC Converters Without Sacrificing Efficiency



This research provides a more thorough understanding of the noise radiation mechanisms in the circuit and proposes innovative solutions to eliminate noise while maintaining circuit performance.

High-speed digital electronic devices, such as computers and cell phones, utilize signals that change rapidly, often on the order of nanoseconds or even picoseconds. These rapidly changing signals are generally transmitted from one integrated circuit to another or to one or more peripheral devices through a network of electrical conductors. The conductors in turn can exist in various forms including cables, wires, circuit board traces, and circuit board planes. However, as the signal transitions become more rapid and occur more frequently, the voltages and currents associated with the transitions can create a weak electromagnetic field in the proximity of the device. The electromagnetic field produced by the device then adds to the ambient electromagnetic fields produced by both natural events (e.g., lightning) and man-made events (e.g., radio and television transmissions). In this way each device contributes to the electromagnetic environment. While the electromagnetic environment is generally imperceptible to the senses, it can be detected with suitable electronic equipment. More importantly, excessive noise introduced into the electromagnetic environment by one device can cause interference to other devices located in proximity. The need is to determine how to design reliable electronic equipment that meets or exceeds regulatory constraints without significantly compromising other important design objectives.

Researchers at the Center for Electromagnetic Compatibility (CEMC) have made a significant technological contribution with their work on reducing emissions from DC-DC converters without sacrificing efficiency. Conventional solutions to reduce noise often reduce the efficiency of the circuit. This breakthrough work conducted at CEMC provides a more thorough understanding of the noise radiation mechanisms in the circuit and proposes innovative solutions to eliminate noise while maintaining circuit performance. A design guideline has been developed and is used during the product design stage to optimize the design of DC-DC converters for minimal radio emissions.

Economic Impact: The design guideline is enabling designers to more quickly optimize the performance of DC-DC converters in various products. Doing so can reduce the number of developmental cycles. This, in turn, substantially reduces developmental costs. Several corporations have implemented this work into a number of products. The guide is helping produce better products at reduced cost to the consumer, and this will help industry realize reductions of electromagnetic emissions from the DC-DC converters that are often used multiple times in each product. Since

DC-DC converters are used in almost all electronic devices, this breakthrough will have profound impacts on the electronic industry. Implications of this work for end-users include reduced cost, fast-to-market product development, and products that are "quiet" to environment while offering improved functionality and performance.

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