Center for the Design of Analog-Digital Integrated Circuits (CDADIC)

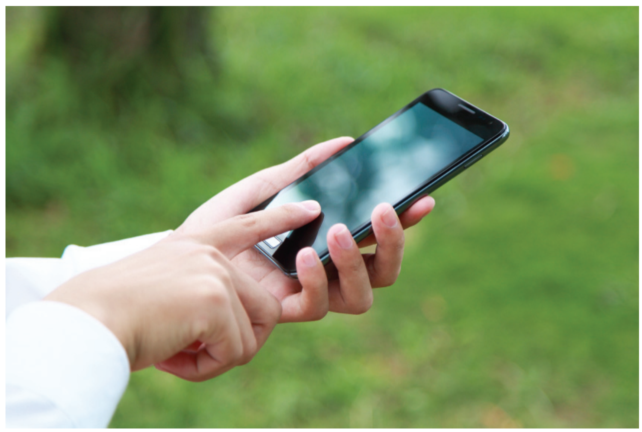
Washington State University, John Ringo, Director, 509.335.5595, ringo@wsu.edu

Oregon State University, Andreas Weisshaar, Co-Director, 541.737.3153, andreas@eecs.oregonstate.edu

University of Washington, Bruce Darling, 206.543.4703, bruced@u.washington.edu

Center website: http://www.cdadic.org/

Noise-Coupled Analog-to-Digital Data Converters

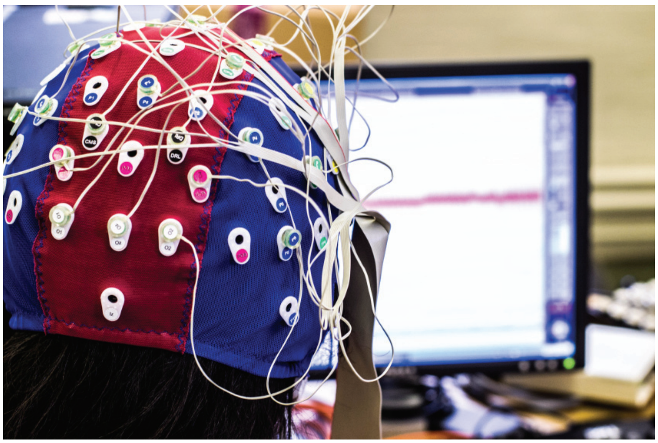


Delta-sigma data converters will result in more efficient cellular phones.

As wireless and wired communication and digital broadcasting proliferate, there is increasing demand for wideband analog-to-digital data converters (ADCs). The signal bandwidth requirement gets more stringent in direct conversion receivers. Along with the wide signal bandwidth, high dynamic range and linearity are also required in these applications. This performance should be achieved in a power-efficient way, since power dissipation determines the battery life for mobile devices. Delta-sigma ADCs can deliver high performance with low-power consumption over wide signal bandwidths, and it is hence the ADC architecture of choice in many wired and wireless receivers. Under a CDADIC-funded project, researchers developed a novel delta-sigma ADC based on noise coupling that provides excellent linearity and power efficiency for wideband communication devices and cell phones.

During 2012, we developed novel data converters based on incremental and extended-counting analog-to-digital conversion. A particularly efficient new configuration was found for extended-counting converters, which multiplexes internal blocks of the circuit. It can achieve lower power dissipation than earlier data converters, and can be shared by many (hundreds) of channels. Hence, they are often the best choice for the interfaces of multi-sensor networks. Such networks are needed in many biomedical and environmental applications.

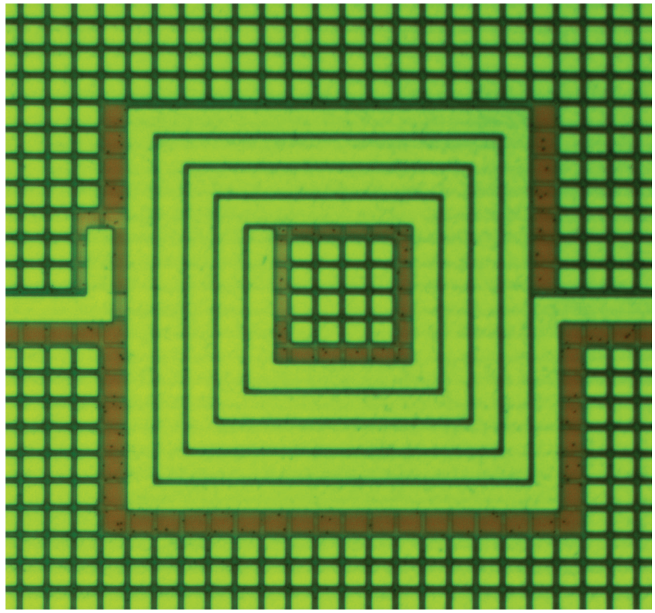
Economic Impact: There is considerable interest at large companies in our results, as shown by gifts received from several CDADIC companies (and many outside ones) to support more research in this field. Noise-coupling converters allow the translation of analog signals into digital form with less distortion and lower power requirements than earlier circuits, and will result in less expensive mixed-mode structures. These have recently been among the most rapidly growing product areas in microelectronics. Since the proposed converters can be shared among many sensors, and require minimal amount of power, they are excellent choices for such applications. Particularly strong economic impacts will be in improved cost-performance ratios of wideband battery-operated systems, including cellular telephones, digital radios, and other wireless devices. Though difficult to quantify, since these products represent a significant percentage of the annual sales of electronic devices, the economic impacts can be anticipated to be substantial. The integrated circuit industry will particularly benefit by this innovation.



The newly developed incremental and extended-counting analog-to-digital data converters are particularly effective in applications involving multi-sensor networks. They are used, for example, in wearable biomedical devices and environmental sensor networks. This photo shows a biomedical sensor network for detecting brain signals.

For more information, contact Gabor Temes, 541.737.2979, temes@eecs.oregonstate.edu.

Enabling Metal-Fill-Aware Design of RF/Mixed-Signal Integrated Circuits



Top view of a fabricated integrated circuit component surrounded by square-shaped metal fills. The metal fills are required by semiconductor foundries to maintain manufacturability and production quality; however, they also impact the electrical performance of the integrated circuit. The impact of metal fills needs to be considered in integrated circuit design.

Semiconductor manufacturers impose strict density requirements for each metal layer in a chip to maintain manufacturability and production quality. To achieve the required minimum density, metal fill is inserted in each layer as needed. The added metal fill can have significant electrical performance impacts on an integrated circuit (IC), especially in high speed or radio frequency (RF) applications. These impacts are not well characterized and have been poorly represented in IC design tools. This research addresses the electrical performance impacts of metal fill on an IC, enabling designers to accommodate and even leverage these effects to their advantage. This work has large potential economic benefits for the US semiconductor industry as well as the US economy at large.

RF designs become extremely sensitive to all electrical effects related to the metal layers at frequencies above 5 GHz. In the past, foundry-imposed metal fill rules have been accommodated for some designs by adding chip area around the perimeter whose only purpose is to increase the percentage of area covered by metal to meet minimum metal density requirements while not impacting the performance of the circuit. The added chip area results in significant waste of silicon, impacting costs and miniaturization. In the drive to add value at decreased cost, the semiconductor industry pushes toward finer and finer geometries, scaling the minimum dimensions of chip-level feature sizes toward fundamental limits. Current and future semiconductor technologies with minimum dimensions of 45 nm and below no longer allow the strategy of increasing chip area to accommodate metal fill density rules while keeping metal fill outside critical areas. Furthermore, each step to a more advanced fabrication process node adds additional cost to both the manufacturing as well as the design of such products. This increases the risk and expense of missing design issues, including that of the impact of metal fill on the functionality and performance of advance products.

This research lays the fundamental groundwork for analyzing and simulating the effects of metal fill on designs to create more robust designs. The results of this research make it easier for designers to plan metal fill placement within the boundaries of a minimum sized chip, while understanding and mitigating the parasitic electrical impact of metal fill and even use metal fill to advantage in their circuit design.

Radio frequency integrated circuits (RFICs) and high-speed digital ICs used in a wide range of end products, including mobile communications and computing devices, will benefit through greater miniaturization, reduced design effort and cost, and improved performance. The performance of phased array antennas for automotive and avionic communications and radar applications should also be improved as a result of this work.

Economic Impact: Semiconductor technology companies will benefit from this work through reduced design effort, improved performance, and greater miniaturization of their RF and high-performance mixed-signal integrated circuit products. In the drive to add value at decreased cost, the semiconductor industry pushes toward finer and finer geometries, scaling the minimum dimensions of chip-level feature sizes toward fundamental limits. Each step to a more advanced fabrication process node, however, adds additional cost to both the manufacturing as well as the design of such products. This increases the risk and expense of missing design issues, including that of the impact of metal fill on the functionality and performance of advance products. This research lays the fundamental groundwork for analyzing and simulating the effects of metal fill on designs to create more robust designs. Furthermore, each mask layer (photomask) in advanced lithographic processes is becoming increasingly expensive; e.g., mask costs for a 28 nm CMOS process are $5 million or even higher. This added expense increases the cost of each design fabrication spin, and increases the emphasis on advanced modeling and simulation capability prior to fabrication.

The design and performance of avionic communications and radar systems should benefit from this research.

The research is expected to strengthen the leadership of US semiconductor technology companies in RF and high performance mixed-signal IC design and manufacturing, which directly impacts the large and growing economic sector of wireless communications with more than $1 trillion in global annual revenues, as well as the important sector of avionic communications and radar technologies. Furthermore, the research should benefit the US automotive industry by improving the performance of automotive radar systems for emerging applications including driver assistance and autonomous driving. This, in turn, will benefit society by potentially saving lives and property through reduced traffic accidents.

For more information, contact Andreas Weishaar, 541.737.3153, andreas@eecs.oregonstate.edu.