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Noise-Coupled Analog-to-Digital Data Converters

As wireless and wired communication and digital broadcasting proliferate, there is increasing demand for wideband analog-to-digital data converters (ADCs). The signal bandwidth requirement gets more stringent in direct conversion receivers. Along with the wide signal bandwidth, high dynamic range and linearity are also required in these applications. This performance should be achieved in a power-efficient way, since power dissipation determines the battery life for mobile devices. Delta-sigma ADCs can deliver high performance with low-power consumption over wide signal bandwidths, and it is hence the ADC architecture of choice in many wired and wireless receivers. Under a CDADIC-funded project, researchers developed a novel delta-sigma ADC based on noise coupling that provides excellent linearity and power efficiency for wideband communication devices and cell phones.

> **Economic Impact:** Noise-coupling converters allow the translation of analog signals into digital form with less distortion and lower power requirements than earlier circuits, and will result in less expensive mixed-mode structures. Particularly strong economic impact may be expected in the cost-performance ratio of wideband battery-operated systems, including cellular telephones, digital radios, and other wireless devices. Since these products represent a significant percentage of the annual sales of electronic devices, the economic affect may be large. The integrated circuit industry will particularly benefit by this innovation.

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Low Voltage Analog Circuits in CMOS

The transistor and voltage scaling are important elements needed in the continuation of digital advancement. While such scaling brings significant advantages to digital circuit design, analog circuit designers face formidable challenges for low-voltage design. This research seeks new ways to overcome these scaling, low -voltage challenges by exploring techniques that will maximize signal swing and compensate for inherent accuracy limitations of analog signal processing. Another important consideration is time and how to make the best use of it. Due to fast transistors that come with scaling, time domain information is becoming more precise. Thus, this research considers ways to trade time information for what has traditionally been utilized as voltage. These efforts have led to novel circuit techniques, such as Correlated Level Shifting that allows signal swing beyond the supply voltage, and Integrating Quantizer that makes use of time domain information to provide an extra order of quantization noise shaping.

> **Economic Impact:** The current and future results from this CDADIC research effort will make higher accuracy and lower power analog/interface integrated circuits possible. With successful advancement in higher accuracy and lower power, meaningful progress will be made in medical applications (hearing aids, pace makers, and other medical devices), emerging consumer markets (high speed and long battery life wireless mobile devices), and other applications (smart sensors, aerospace, military).

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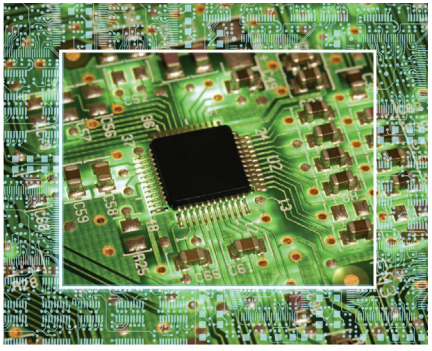
Low-power Data Converters

Data converters provide the translation between the analog signals of the real world and the digital signals processed by computers. Hence, they play a key role in cellular telephones, digital television, CD and DVD players, and many other telecommunication and consumer electronics applications. More recently, data converters also are playing increasingly complex and demanding roles in diagnostic medical devices used in EKG, EEG, ultrasound monitors, hearing aids, brain stimulators, and other applications. In such applications, in addition to the usual requirements for speed and accuracy, low power dissipation plays a crucial role, since often power is supplied by batteries, or scavenged from the environment. This research has resulted in important technological advances in this field.



Economic Impact: CDADIC researchers have been successful in finding novel architectures and algorithms that provide excellent trade-offs between accuracy, speed and power requirements of low-power data converters. Research results from this work are being incorporated into the design of multi-sensor networks used to monitor brain waves, heart beats and other biomedical signals.

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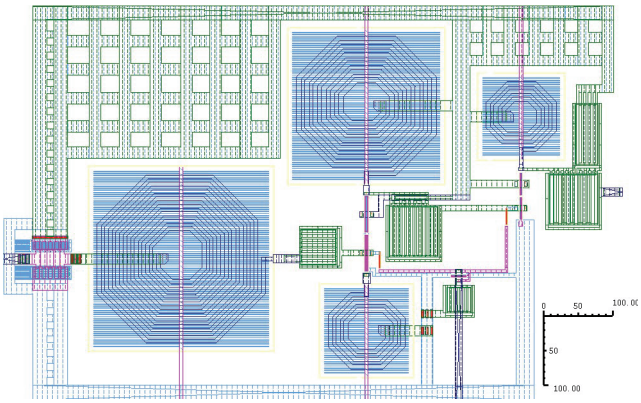
Modeling and Design of Integrated Circuit Protection Systems



CDADIC research has led to the development of new circuit designs and new compact modeling methods for protecting integrated circuits against the effects of electrostatic discharge (ESD) and electrical overstress (EOS). These problems have most commonly been dealt with using a trial-and-error method, but new compact models and simulation tools can now predict the current pathways on a chip that an ESD or EOS pulse will take, and then evaluate the robustness of the design to dissipate the energy of the errant pulse. This can eliminate much of the guesswork in ESD/EOS design, and can help bring products to market faster by evaluating ESD/EOS robustness prior to fabrication. ESD protection is also particularly difficult for sensitive RF circuits. New circuit protection systems for RF front-end circuits are also being designed, such as those used in cell phones and other wireless systems. ESD/EOS protection is predicted to become an even greater challenge for the newest generations of 22 nm and 16 nm CMOS processes. Thermal effects in these devices are also being studied to better predict the energy dissipation tolerance and their susceptibility to ESD/EOS transients. This will lead to improved simulation models and better ESD/EOS tolerant designs.

Economic Impact: Approximately 0.5 percent of all integrated circuits fail, and of these failures, approximately two-thirds of those are caused by ESD/EOS. For the annual worldwide semiconductor industry market of around $300B, ESD/EOS failures thus constitute roughly a $1B annual problem. The most demanding environments for ESD/EOS stresses involve analog, mixed-signal, and RF integrated circuits, for which the simulation tools have the least well developed circuit models. ESD/EOS protection systems for these types of ICs necessarily require a greater level of customization, and accurate ESD/EOS circuit simulation can play a significant role in producing more reliable IC designs.

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PIN-Diode-Based Phase Shifter in Silicon Germanium

Phased array antennas (PAAs) are critical for next-generation satellite radios, broadband Internet, and GPS systems. A PAA consists of tens-to-thousands of individual, identical antenna elements. Each element consists of an antenna or radiator and associated electronics that amplify and phase shift the signal at each element. The primary factor limiting broader usage of PAAs has been their high cost, which is driven by the cost of the element electronics. This CDADIC research has successfully reduced the cost of an important electronic functional block used in each PAA element, the phase shifter. Working with one of CDADIC's aerospace partners, center researchers have developed and modeled a PIN diode switch in silicon germanium (SiGe) Bi-polar/Complementary Metal Oxide Semiconductor (BiCMOS) technology. They have included this switch in an integrated, high-performance phase shifter. Over the years, this team has enhanced the linearity, isolation, and loss performance of the PIN diode and applied the improvements to implement multiple-channels and multi-beams, resulting in an integrated, light weight, and low power solution for PAAs. This has enabled the development of fully-integrated PAA electronics in a single SiGe BiCMOS integrated circuit. The result is lower cost PAAs, with higher performance.

Economic Impact: Based on these research results, The Boeing Company is now using the developed technology to implement various beamformers in defense and commercial applications based on the PIN diode phase sifter for high linearity. Linear Signal, Inc. is also using this research for various high performance beamformers based on the PIN diode phase shifters in silicon technology and providing these results to its customers in the commercial and defense domains. These low cost electronics will dramatically lower the cost and enhance the performance of mobile satellite television and internet for laptops, automobiles, boats, aircraft, and more. They will also introduce true reliable (SLA) services from satellite providers by providing self-correcting antennas that can repoint to backup satellites during transponder saturation or even thunderstorms.

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Coupling Suppression in Integrated Circuits using Dummy Metal Fill

Metal fill is required by semiconductor foundries to achieve planarization of the dielectric and metal layers. The added metal fill can have electrical performance impacts on an IC, especially in high speed or RF applications. These impacts are not well characterized and captured in IC design tools. This project addresses these issues, enabling designers to accommodate and even leverage these effects to their advantage.

Phased array antennas for communications and radar applications should be improved as a result of this work.

RF designs become extremely sensitive to all parasitic effects related to the metal layers at frequencies above 5 GHz. In the past, metal fill rules have been accommodated for some designs by adding chip area around the perimeter whose only purpose is to increase the percentage of area covered by metal to meet metal fill rules. This results in significant waste of silicon, impacting costs and miniaturization. This research makes it easier for designers to plan metal fill within the boundaries of a minimum sized chip, while understanding the impact of the metal fill and even the associated parasitic effects to advantage in their circuit design.

RFICs and high-speed digital integrated circuits used in a wide range of end products will benefit through greater miniaturization, reduced design effort and improved performance. Phased array antennas for communications and radar applications should be improved as a result of this work.

> **Economic Impact:** Semiconductor technology companies will benefit from this work through reduced design effort, improved performance, and greater miniaturization of their RF and high-performance mixed-signal integrated circuit products. The research is expected to strengthen the leadership of US semiconductor technology companies in RF and high performance mixed-signal IC design and manufacturing, which directly impacts the large and growing economic sector of wireless communications.

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Low-Cost MIMO Transceivers Using CMOS Technology

CDADIC researcher Dave Allstot is developing low-cost multiple-input multiple-output (MIMO) transmit/receive systems on monolithic microwave integrated circuit (MMIC) chips based on fine-line CMOS technology. Such systems traditionally have been implemented using gallium arsenide technology, which is more expensive and won't support putting the multiple transmitter, receiver, and control functions on the same integrated circuit. Phased array transceivers, used in aerospace and satellite communications, for example, use a radio channel for each element of the array. The cost limits how widely the technology gets used. Moreover, extensions of basic MIMO techniques are attractive for emerging cognitive radio systems. This research should help dramatically increase the use of MIMO transceivers in applications that are critical to the military for DOD's next-generation communications.

> **Economic Impact:** MIMO transmit/receive systems have now become a mainstream production technique in CMOS radio frequency, integrated circuit design and production. Many of the techniques associated with this research, are used by high technology companies throughout the world in CMOS radio chips and are having major economic impacts.

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