Center for the Design of Analog/Digital Integrated Circuits (CDADIC)

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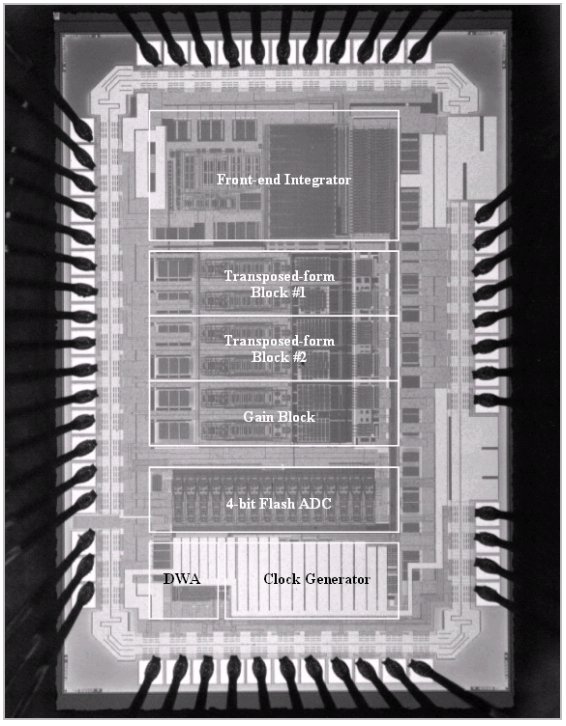
New Integrated Circuit Technique: Output Prediction Logic

At CDADIC, University of Washington electrical engineering professor Carl Sechen is currently designing and implementing the world's fastest digital logic technique. This ultimately will allow for significant increases in chip speed. Sechen's Output Prediction Logic (OPL), a new integrated circuit technique that was recently patented, will double the speed of existing methods of computing digital logic functions on a chip. Eventually, this technology will make it possible to double computer speed as well as greatly enhance video and speech processing technologies. Sechen has already made considerable progress in the area of computing circuit design for speech recognition, an area that requires much faster computer chip capability than currently exists. The high-speed logic design methods and libraries that Professor Sechen has been working on will, for example, allow Boeing for the first time to implement the STAP (Space-Time Adaptive Processing) algorithm on a single silicon integrated circuit. Boeing will be able to process imaging data using that algorithm at previously unachievable speeds in a small space and at acceptable power levels. The STAP algorithm, running at those speeds, will enable data filtering and clutter reduction at unprecedented levels. If successfully implemented, this algorithm has been targeted for adoption by several high-visibility defense applications and will become truly breakthrough/enabling technology to the associated programs. For more information, contact Carl Sechen, 206-685-8756; e-mail: sechen@ee.washington.edu.



Circuit Protection Modeling Systems

University of Washington electrical engineering professor Bruce Darling is developing compact circuit simulation models that predict the effects of electrostatic discharge (ESD), a problem of major concern in modern microelectronics. As integrated circuits become more dense and miniaturized, they become more fragile and susceptible to damage by static electricity. Previously, the design of ESD circuit protection has largely been a trial-and-error process and, consequently, the introduction of new product design has been slow and difficult. Darling's novel research takes the guesswork out of this process. He and his Ph.D. student, Yeshwant Subramanian, are developing software tools that identify the pathways that an ESD current pulse can take within the layout of an integrated circuit, and predict the effects of this pulse on the semiconductor devices that it passes through. By simulating many possible ESD events before they happen, industry will be able to understand the robustness of a given design prior to fabrication, and be able to produce more reliable, secure integrated circuits. This will allow new products to move on to the market more quickly and more economically. For more information, contact Bruce Darling, 206-543-4703; e-mail: bdarling@ee.washington.edu.

Low-Cost Phased Array Antenna Using Silicon Germanium Technology

CDADIC researcher Dave Allstot is developing a low-cost phased array transmit/receive system on a monolithic microwave integrated circuit (MMIC) chip based on silicon germanium technology. Such systems traditionally have been implemented using gallium arsenide technology, which is more expensive and won't support putting the transmitter, receiver, and control chip on the same integrated circuit. Phased array antennas, used in aerospace and satellite communications, for example, use MMICs for each element of the array. The cost of the MMICs is a large factor in the cost of the antenna, which limits how widely the technology gets used. This research should help dramatically increase the use of phased-array antennas in applications that are critical, for example, to the military for DOD's next-generation battlespace communications. For more information, contact Dave Allstot, 206-221-5764; e-mail: allstot@ee.washington.edu.

Delta-Sigma Toolbox Enhances the Design of Data Converters

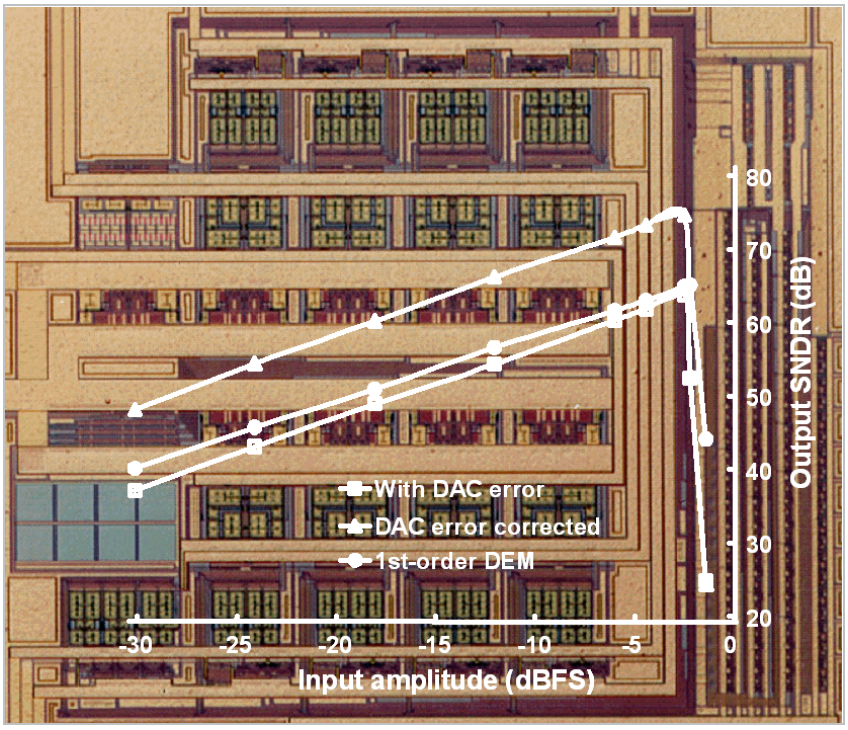
The Delta-Sigma Toolbox is a tool developed at CDADIC and made available to the general public that allows engineers to explore "What if" scenarios in designing Delta-sigma over-sampled data converters, one of the most important of all general architectures in the conversion of real world signals (analog) to data manipulation signals (digital). With this tool, engineers can quickly explore the effects of arranging converters in different configurations. Analog Devices, a CDADIC industry partner, is one company that has made extensive use of this tool over the years and has saved a tremendous amount of time trying to figure out the best way to make these converters. The tool is used by thousands of engineers in the United States. For more information, contact Richard Schreier at richard.schreier@analog.com.

Changes in Analog/Digital Converters

CDADIC researchers have developed current-mode logic circuits for low-noise performance. The technology provides a way to reduce digital substrate noise in mixed-mode integrated circuits, which has been a major limitation of the accuracy achievable in such circuits. Digital switching noise is a potential problem in the design of analog/RF/digital system-on-chip (SoC) solutions. At high frequencies, the sensitive analog/RF circuits are unable to reject substrate-coupled switching noise. Current-mode logic circuits were invented to overcome this problem; they generate

switching noise that is more than two orders of magnitude less than that of conventional static logic circuits. The proposed digital design methodology in SoC solutions is to use conventional logic for low-frequency functions and low-noise current mode logic for high-frequency functions. Although it dissipates DC power, current-mode logic is actually more power efficient at high frequencies. To date, the current mode logic has been used in the frequency divider blocks of phase-locked loops wherein it provides superior jitter performance. Several semiconductor companies have used the logic techniques in these applications. For more information, contact Sayfe Kiaei, 480-727-7761; e-mail: sayfe.Kiaei@asu.edu, or David Allstot, 206-221-5764; e-mail: allstot@ee.washington.edu.

Advances in Analog/Digital Converters



An analog-digital converter (A/DC) is a mixed-mode integrated circuit, composed of both an analog and digital component. This type of circuit is essential in applications where the two different signals are required, such as in cell phones, camcorders, and hearing aids. A/DCs are needed to convert real-world analog signals, such as sound waves, into digital format, where information is represented by numbers allowing data to be stored and processed. There is constant demand to increase the accuracy and speed of A/DCs, as well as gain efficiencies in power consumption. CDADIC researchers at Oregon State University (OSU) are advancing the state-of-the-art in A/D converter technology, especially in the areas of low-voltage operation, compatibility with low-cost digital CMOS processes, and high throughput delta-sigma ADCs. These are important advances that are pushing the limits of the current technology in this field. Extending the performance window for A/D converter technology will ensure that there will be A/D architectures that will be compatible with next generation IC processes.

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