An Autonomous Evolvable Architecture in a Reconfigurable Protocol Chip for Satellite Networks

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Introduction

NASA's Earth Science Enterprise Strategic Plan [1] and Research Strategy for 2000-2010 [2] identify satellite constellations, distributed spacecraft, and formation flying technologies as an important technology thrust and investment areas, applicable to a range of NASA missions. Such missions will have wireless network protocols derived or extended from commercial efforts in this area. Commercial protocols or modified versions may find their way into many future distributed spacecraft missions. It is challenging to find one "universal" protocol to meet the requirements of all of these future missions. This being the case, missions in the next 5-10 years are extremely likely to be operating with multiple protocols and substantial protocol variations depending on the requirements of the distributed spacecraft mission.

Figure 1.a is a notional illustration of network nodes that will operate in distributed spacecraft missions with heterogeneous networks, and Figure 1.b illustrates the network nodes operating in a heterogeneous network.

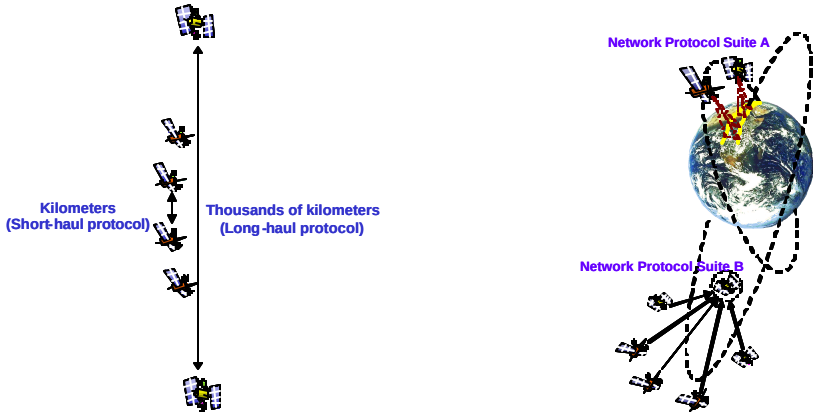

Figure 1.a-b Notional illustrations of distributed spacecraft mission with different protocols and mission with heterogeneous nodes/protocols, respectively.

This paper will present the architecture for a space-based dynamic reconfigurable protocol chip (RPC) for Earth Science Enterprise satellite constellations. In order to improve dependability, Concurrent Error Detection (CED) techniques are considered and a two tiered architecture is presented for two link layer protocols, HDLC and IEEE 802.3 (Ethernet).

Brief Summary Related Work and References

A prototype development is underway at the Jet Propulsion Laboratory (JPL) that will demonstrate the autonomous protocol detection and autonomous reconfiguration of the RPC in a heterogeneous network. Technologies developed will target future satellite constellations and applicable to the CALIPSO mission, flying in formation with Aqua (2004), COACH (2006), EOS-9 Global Precipitation Mission (2007), and Grace follow-on: formation flying spacecraft (2010). They also conform fully to technology thrust areas described in the Earth Science Enterprise Strategic Plan. Error detection schemes for reliability in Xilinx circuitry can be found in [3],[7]. Fault location techniques have been addressed in [4].

References

[1] Earth Science Enterprise – Strategic Plan, http://www.earth.nasa.gov/visions/stratplan/index.html
[2] Earth Science Enterprise – Research Strategy, http://www.earth.nasa.gov/visions/researchstrat/Research_Strategy.htm
[3] The Reliability of Data Program, http://www.xilinx.com/products/qa_data/relreprt.pdf
[4] W. Huang, et. al., "Fast Run-Time Fault Location in Dependable FPGAs", IEEE ITC 2001, Oct 30-Nov1, Baltimore, MD, http://www-crc.stanford.edu/crc_papers/huangitc01.pdf .
[5] http://www.xilinx.com/ipcenter/hdlc/
[6] http://www.xilinx.com/ipcenter/catalog/search/alliancecore/cast_mac.htm
[7] R. Karri, et. al., "Concurrent Error Detection architecture for symmetric block ciphers", MAPLD 2000.

Discussion of Key Elements in Paper

In this paper we present an overall architecture for a reconfigurable protocol chip to be used in Space-based applications. The reconfigurable protocol chip comprises of a sensing and detection module, a reconfiguration control engine, a protocol selection module, and the selected protocol as depicted in Figure 2.

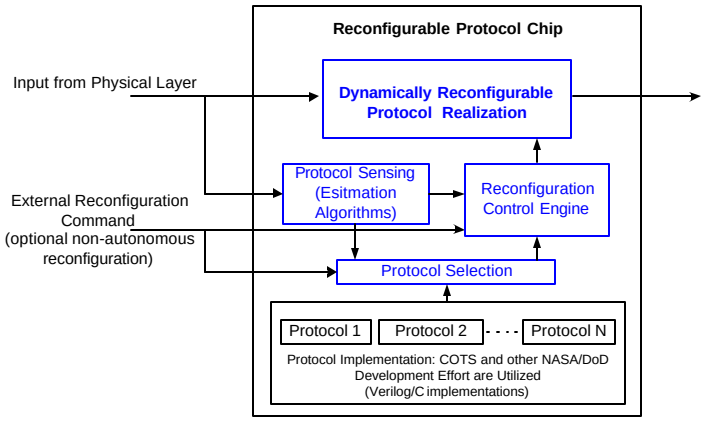

Figure 2. Block Diagram of the internal architecture of the reconfigurable protocol chip

We then present a two-tier reliability architecture as depicted in Figure 3 below. In Figure 3 we present an example of 4 pre-compiled version of the FPGA core with constrained routing. Specifically the circuit with error detection circuitry is compiled eliminating the upper left quadrant (Purple), the upper right quadrant (Orange), the lower right quadrant (Blue) and the lower left quadrant (Brown). To insure the error detection circuit in the FPGA is operating properly, the second tier operation, called the CED checker provides a redundancy on error detection.

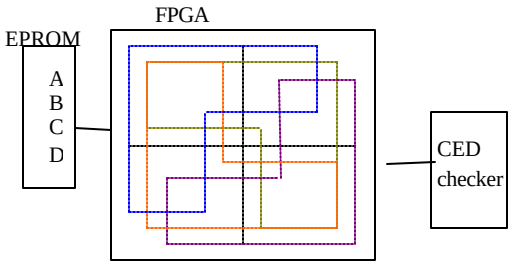

Figure 3. Two tier reliability architecture example using redundant computation for error detection.

We then examine trades for High Level Data Link Control (HDLC) and IEEE 802.3 core logic [5][6]. We consider the HDLC operating at the data link layer where data is encapsulated in an HDLS frame containing an HDLC address and control field followed by a Cyclic Redundancy Check (CRC) code used for detecting errors in the transmission. Ethernet, also known as IEEE 802.3 is referred to as the Logical Link Control (LLC) protocol as is based on HDLC. LLC uses as extended 2-byte address where the first address byte indicates a Destination Service Access Point (DSAP) and the second address indicates a Source Service Access Point (SSAP). We then present results with integrated CED schemes similar to [7] and perform trade analysis for the area overhead as well as the overhead due to redundant constrained precompiled core.

Conclusion

We presented a reconfigurable protocol chip architecture for space-based application. We then presented a two tier architecture for autonomous adaptation combating circuit failures and then identify the trades for using improving reliability for autonomous repair in a reconfigurable protocol chip platform.