1. Description of the Solid State Telescope Analogue Electronics Box (SSTA).

1.1 Brief description of the SSTA operation.

The main function of the SSTA is to convert the signals received from the F and O detectors into digital data words which are then transferred to the memory buffer located in the Data Processing Unit (DPU).
Fig.1 (p.4) shows the simplified block diagram of the analogue part of the instrument.

The Charge Sensitive Amplifier (CSA) signals are first shaped into Gaussian pulses in pulse shaping amplifiers with approximately 900 nsec pulse shaping time constant.
The peak values are then sensed and stored by peak-detector-sample-and-hold circuits (PDSH) until they are digitised by two 8 bit analogue-to-digital converters (ADC) which convert the F and O signals respectively.

The 8 bit data (256 levels) are compressed into 16 energy channels (for the F data) or 24 energy channels (for the O data) before transfer to the DPU.
The maximum conversion rate of the ADCs is about 150 Kcps (conversion time = 6.6 μsec).

All events detected in each channel above the noise threshold (fixed by discriminators) are accumulated in 24 bit counters read out serially to the DPU together with operating status parameters.

In normal operating mode, or "Measure" mode, only signals originating from one detector of a pair are analysed. Any penetrating event is rejected by the other adjacent detector.

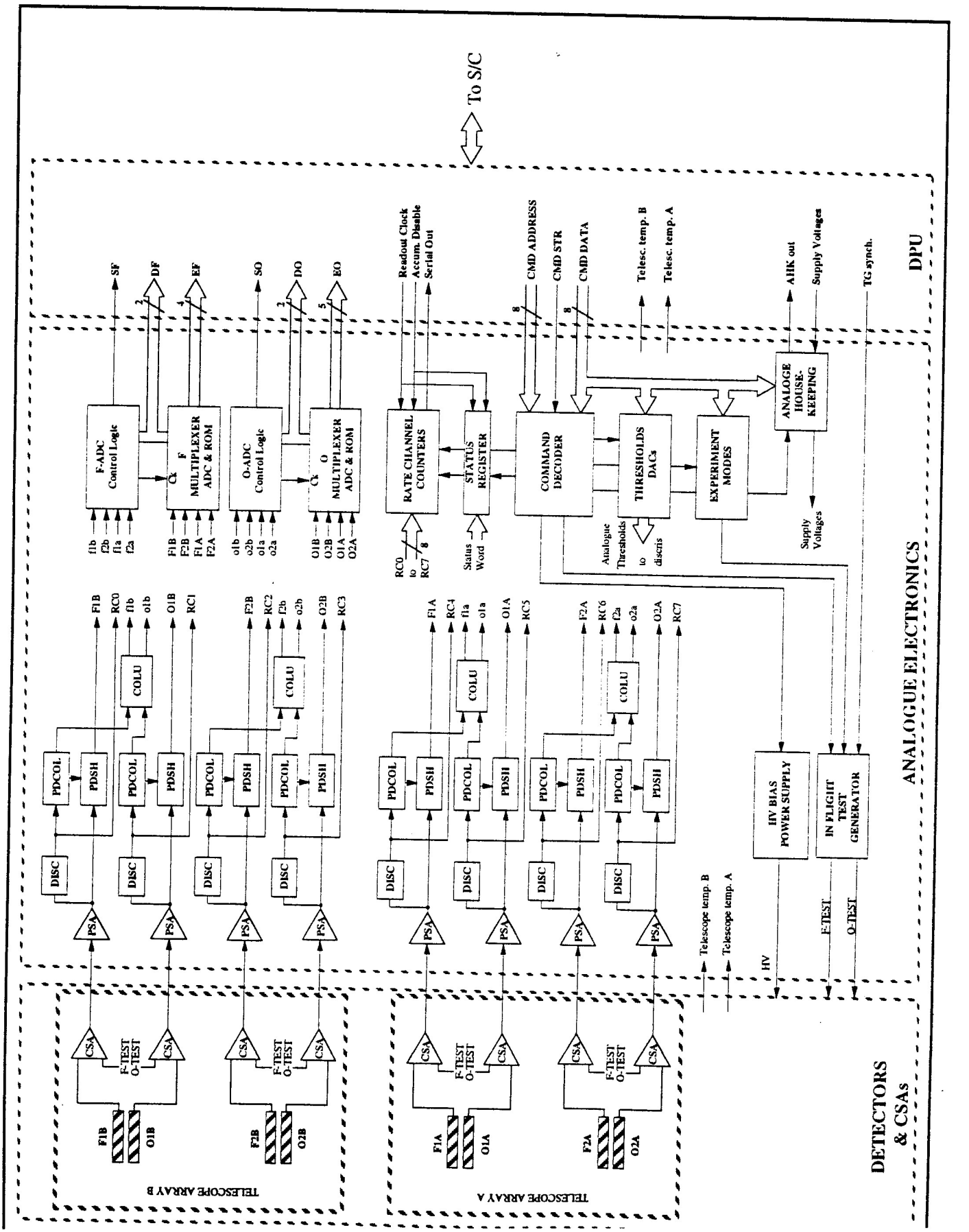
Besides the "Measure" mode the experiment can be switched to 8 other operating modes by command, which are used for test and calibration.

Auxiliary functions, performed under command from the DPU, are :

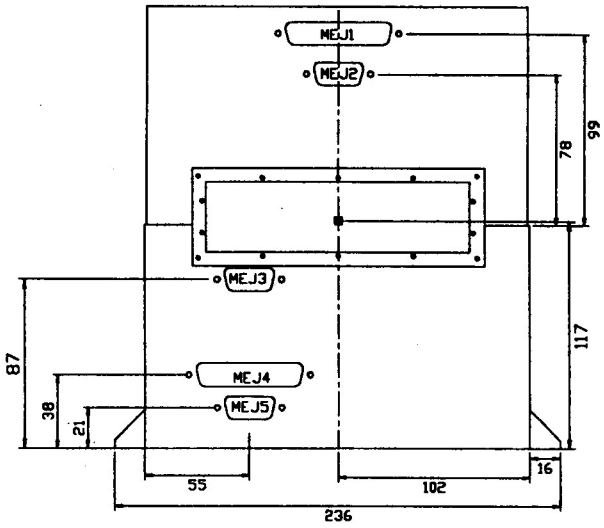
- control of the detector bias voltage
- control of the discriminator thresholds
- control of the internal test generator
- analogue housekeeping read out to the DPU (supply voltages and currents, temperature of electronic circuits).

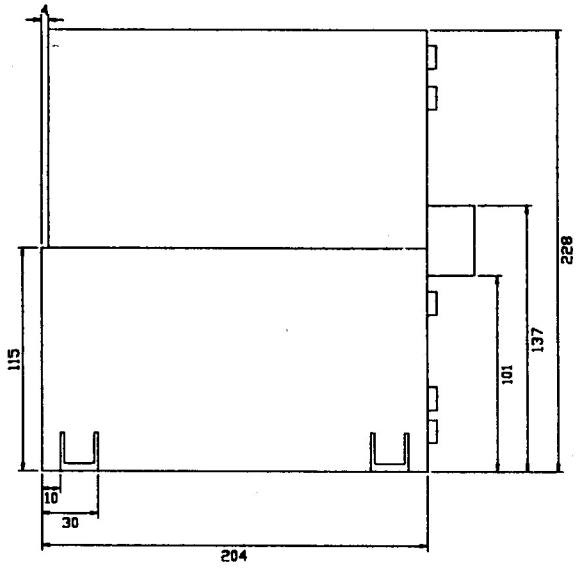
Fig. 1 - EQUATOR-S SST ANALOGUE ELECTRONICS

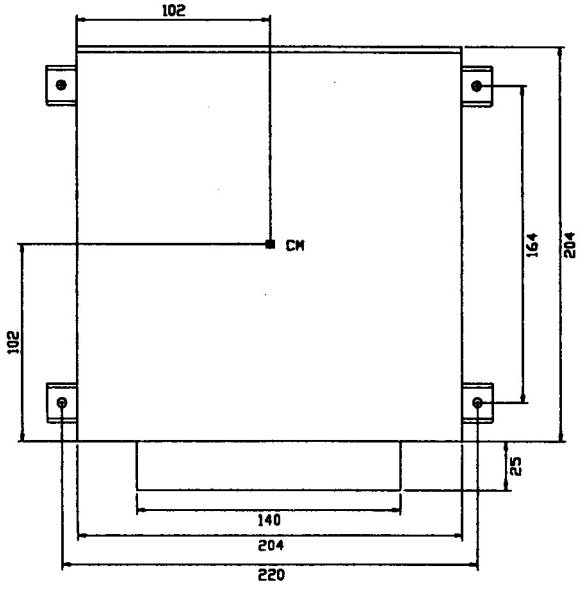
SIMPLIFIED BLOCK-DIAGRAM REV. 7b (1 May 1996)



DPU/SST Analog ICD Drawing







Component	Mass(kg)	Power(W)
DPU	5.0	3.9
SST Analog	3.6	3.8

Connector Id	Type	Function
MEJ1	MCDM3-17S	SST Coax
MEJ2	DAM-15S	SST Interface
MEJ3	HD20-15S	Command/TM
MEJ4	DCM-37S	Analyzer Interface
MEJ5	DAM-15P	Power Interface

MATERIAL	DRAWN	DATE	TITLE	SHEET	
	McCarthy	14-Mar-95	DPU/SST Analog ICD Drawing	1/1	SPACE SCIENCES/GEOPHYSICS
FINISH	ISSUED	SCALE - DO NOT SCALE -	DRAWING NR.	REVISION	UNIVERSITY OF WASHINGTON
Black Anodize finish		1:4	EQSICD3	1.1	SEATTLE, WA 98195 (206) 685-2543

2.2 SSTA/DPU input and output interfaces.

2.2.1 Digital input interface circuit.

The SSTA logic uses CMOS or High Speed CMOS supplied under +5.1V.
The diagram of Fig. 2 shows a typical input circuit of the SSTA.

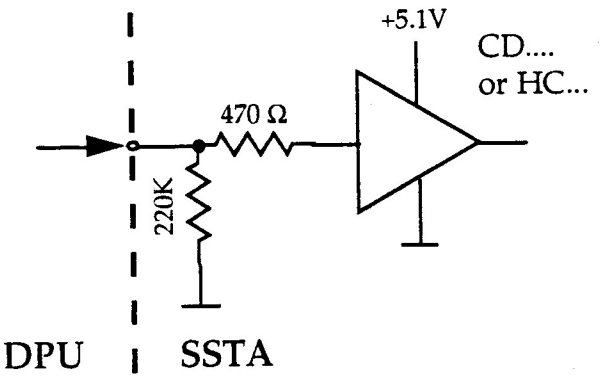


Fig. 2 - Digital input interface circuit.

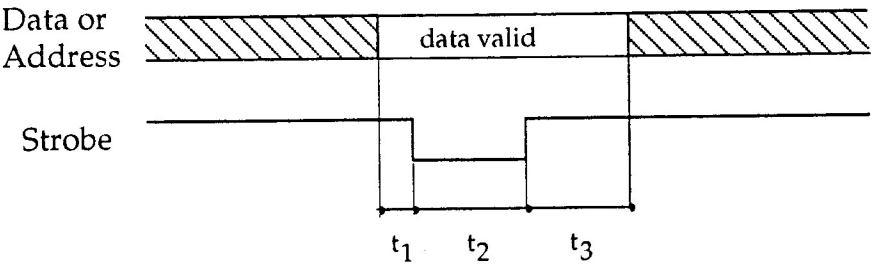
2.2.2 Digital input signals.

The SSTA digital signals received from the DPU are :

- parallel 8 bit Command Data word
- parallel 8 bit Command Address
- Command Strobe
- Internal Test Generator synchronisation clock
- Serial Data shift clock
- Serial Data parallel/serial control (Counter Disable\)

2.2.2.1 Command signals.

The data and address parallel 8 bit words are latched in the command decoder on the leading edge of the Command Strobe signal (1 µsec min. duration, active low). Fig. 3 shows the command signals timing.



t_1 = 200 nsec min.

t_2 = 1 µsec min.

t_3 = 1 µsec min.

Fig. 3 - Command signals timing diagram.

2.2.5 Analogue input circuit.

2.2.5.1 Analogue input interface circuit.

All 8 Pulse Shaping Amplifier (PSA) input circuits are identical (Fig. 7).
They require negative input signals from the CSAs.
The input impedance is approximately 1 kΩ.

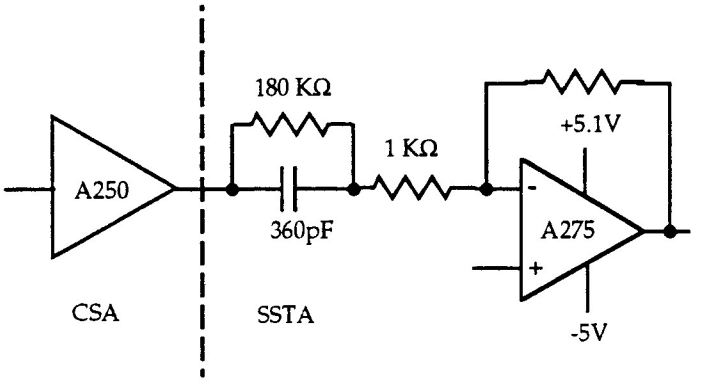


Fig. 7 - PSA input circuit.

2.2.6 Analogue output circuit.

2.2.6.1 Analogue housekeeping output circuit.

The analogue housekeeping circuit delivers the monitored parameters in the range of +4V to -4V.

The diagram of Fig. 8 shows the analogue housekeeping output circuit.

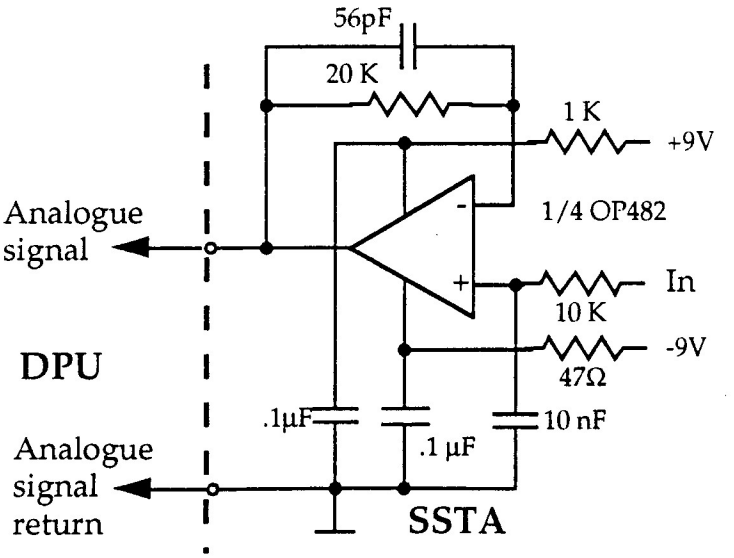


Fig. 8 - Analogue housekeeping interface circuit.

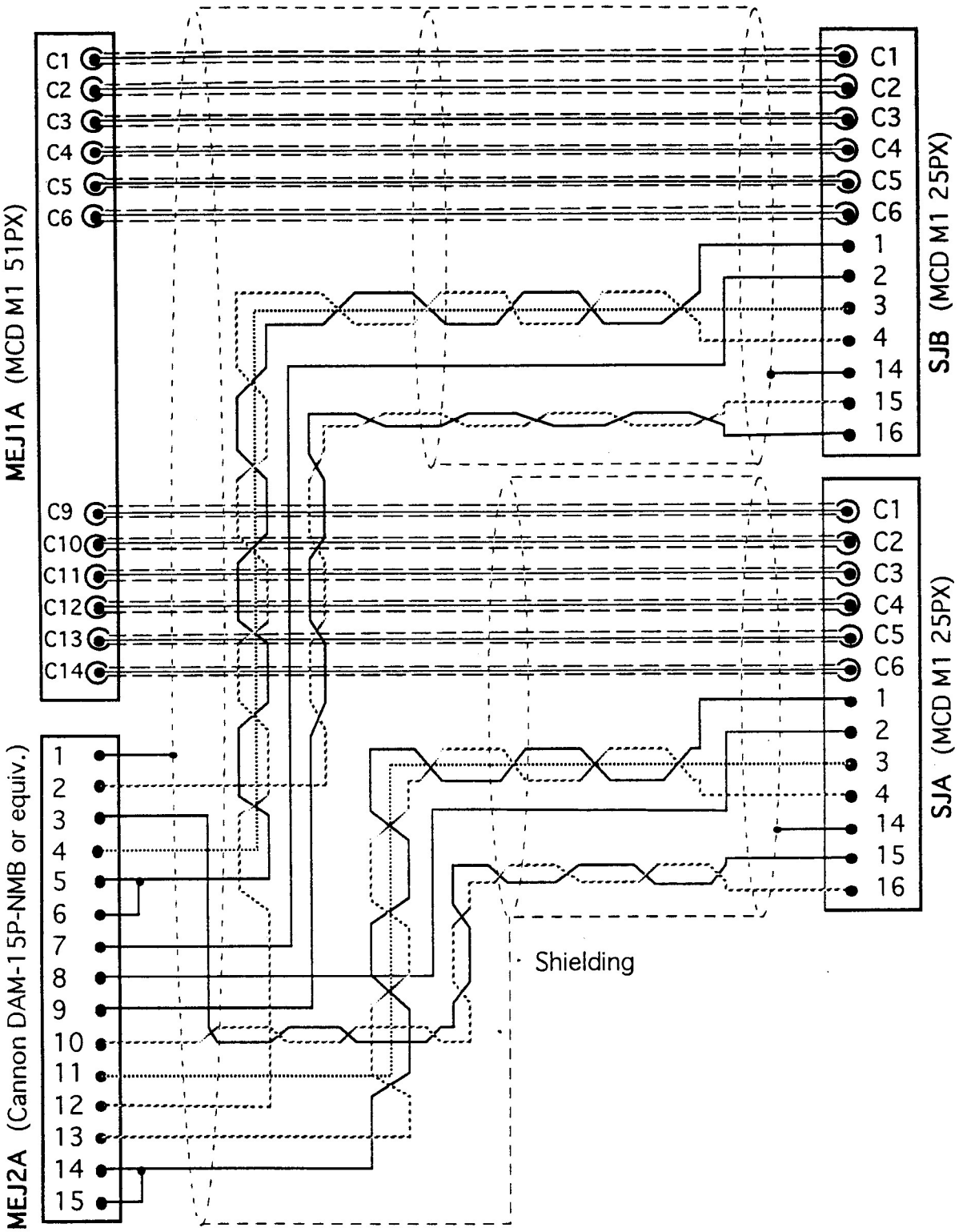


Fig. 18 - SSTA/telescope harness block-diagram.