Transactions Briefs

A 12-Gb/s DEMUX Implemented With SiGe High-Speed FPGA Circuits

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***Abstract*—A 7–12-Gb/s demultiplexer implemented with circuits for a high-speed field-programmable gate array (FPGA) is introduced in this paper. Since the first FPGA was released by Xilinx in 1985, FPGAs have become denser and more powerful. The first FPGA that operates in the microwave range was designed in 2000. Various methods, such as a new basic cell structure and multimode routing, are used to make that design faster and less power consuming. Sequential logic functions are analyzed and tested in this paper with a DEMUX implementation using these high-speed FPGA circuits. A chip measurement has shown that the FPGA can operate at a 12-GHz system clock when configured to perform sequential logic. A DEMUX that operates at 12 Gb/s is used here to demonstrate the potential for high-performance and low-power FPGA features.**

***Index Terms*—Current mode logic (CML), field-programmable gate arrays (FPGAs), programmable logic arrays, silicon germanium.**

I. Introduction

Field-programmable gate arrays (FPGAs) are being employed more often in high-speed networking, prototype circuit design, and digital signal processing. While CMOS FPGAs are struggling with gate delays and dynamic power consumption, an alterative high-speed FPGA was first introduced in 2000. This first gigahertz range FPGA utilized state-of-the-art SiGe high performance (HP) BiCMOS technology and current mode logic (CML) to implement the Xilinx XC6200 series basic cell at 5 GHz [2]. CML circuits are continuously power–hungry, so new methods must be deployed to reduce power consumption, increase performance, and provide more functionality when possible. Circuit tricks are described in this paper to provide a feasible high-speed FPGA chip. Several chips have been fabricated by the IBM 7HP BiCMOS process. The measured gate delay through a single basic cell is as small as 100 ps. The measured DEMUX, which is implemented by this FPGA, can have a maximum data throughput of 12 Gb/s.

This paper chooses the IBM SiGe 7HP BiCMOS technology for the FPGA design. SiGe technology has speed advantages over the traditional Si technology [2]. SiGe technology was first introduced by IBM in the 1980s [3] and has evolved through eight mature generations to reach cutoff frequencies of about 120 GHz for the 7HP process and 210 GHz for the 8HP process [4].

Section II briefly reviews the high-speed FPGA. Three methods are utilized to increase functionality, reduce power consumption, and improve circuit performance. As an example of many possible applications, a DEMUX is implemented with this high-speed FPGA to demonstrate the sequential logic function. Circuit details and measurement results are shown in Section III and conclusions are stated in Section IV.

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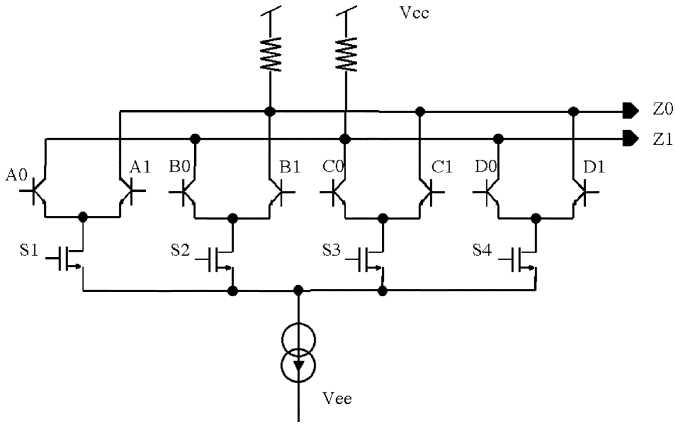

Fig. 1. Newly designed 4:1 MUX. Each BJT pair can be turned on/off separately. An 8:1 MUX will not require a higher voltage than a 2:1 MUX. A MUX can be completely turned off in this design [7].

II. High-Speed FPGA Design

A. Introduction

The high-speed FPGA utilizes the XC6200 architecture as the starting point for the initial design. The XC6200 series are multiplexer-based FPGAs designed for digital signal processor (DSP) applications. They are open source in both the hardware and software domain. As shown in [5], multiplexer-based FPGAs have speed advantages over look-up table (LUT)-based FPGAs. It is also easier to convert multiplexer-based FPGAs into CML than LUT-based FPGAs.

Even CML has its own limitations. The original CML version of the XC6200 basic cell consumed 62 mW. Total basic cell power consumption was 16 W in a 16×16 gate array. Besides the high-power consumption, lack of routing resources also limits the application of that gigahertz FPGA. The FPGA described in [7] and [8] has a dramatic improvement on the power consumption and routing capability by using new multiplexers, a new basic cell structure, and a multimode routing method. Measurement results have shown that the combinational logic of the FPGA has a delay as short as 100 ps. The methods used to improve the FPGA are reviewed briefly in the following.

B. New Multiplexers

Fig. 1 shows an alternative MUX used in the FPGA compared with [1] and [2]. This new MUX uses a one level selection tree. A user can select which current is to be turned on. Otherwise, a user can choose

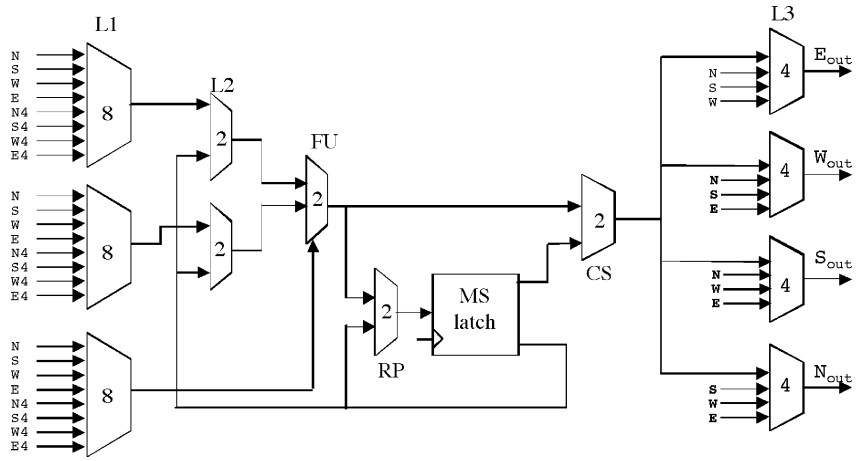

Fig. 2. Basic cell that is used in XC6200. Each output is selected by the output multiplexer (L3) and combination/sequential multiplexer (CS). One input signal passes five multiplexers. Each basic cell provides one output in each direction.

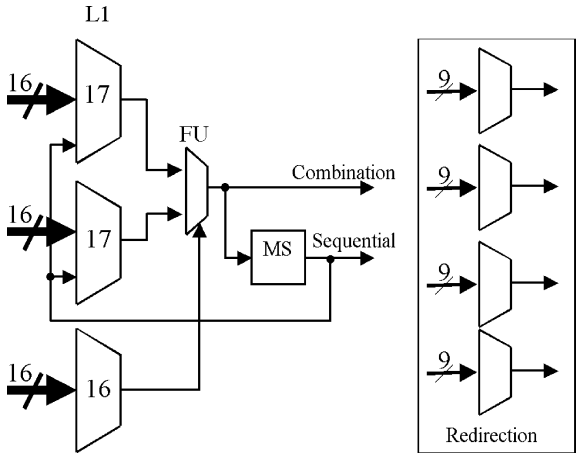

Fig. 3. Improved basic cell II. In the BCII, combinational, sequential and redirection outputs are separated. This structure provides the most routing capabilities and least gate delays.

to turn off the MUX by turning off all the NFETs. The system voltage can be as low as 2.8 V, saving a significant amount of power.

In addition to the lower power and the selective off features, more versatile MUXs can be implemented. No longer do the MUX inputs need to be a multiple of 2. For example, a 9:1 MUX used in this paper can be implemented by using this structure.

C. New Basic Cell Structure

A regular basic cell that is used in XC6200 series is shown in Fig. 2. An improved basic cell II (BCII) is shown in Fig. 3.

In the BCII, instead of being selected by CS and L3 MUXs, combination, sequential, and redirection results are sent directly to a cell's neighbor. Each cell provides three outputs to its neighbors in one direction instead of just one output. Consequently, the L1 MUX will receive a total of 16 inputs in all 4 directions. In each direction, three inputs from neighbor cells and one input from the FastLANE. The first two L1 MUXs also have an extra feedback input from the MS latch. That requires the first two L1 MUXs in the BCII be two 17:1 MUXs. In practice, the gate delay of a 16:1/17:1 MUX is longer than a two-level 16:1/17:1 MUX. In this BCII, the 16:1 MUX is implemented by five 4:1 MUXs; four MUXs on the front end and one MUX on the back end.

Without the logic function results, the L3 MUX in the previous design is transformed into a redirection MUX, which only relays signals of neighbors. Since each neighbor provides three inputs, the redirection MUXs have been changed to four 9:1 MUXs.

The advantage of the BCII is obvious, a signal passes through three MUXs instead of five: two-level L1 MUXs and an FU MUX. The total gate delay is only 60% of the previous design and all the logic functions are preserved. Besides the performance improvements, more routing capability is provided by this new design. A cell has more choices to pick from instead of just one.

D. Multimode Routing

High power consumption is the main disadvantage of CML. In this BCII design, a multimode routing method is used to reduce power consumption. This method can be best described as turning off unused cells and current tree in an application. At the system level, if an application uses 10 cells in a 4×4 gate array, turning off the six unused cell saves about 40% power. At the cell level, turning off unused CML trees has a similar contribution to total power savings.

For example, when a basic cell only uses its combination logic function; the MS-Latch and redirection multiplexers are turned off to save power.

Besides sequential logic circuits, more circuits can be turned off in the normal mode. Each BCII needs two signals to generate a logic function. Therefore, at least two output-drivers or two redirection multiplexers in its neighbor cells may be turned off to save power. When a cell's input signals are selected from the FastLANE, all four output-drivers in all neighbor cells may be turned off to save power.

When a cell is configured to redirect a signal from one neighbor cell to another neighbor cell, only the redirection multiplexer needs to be turned on. Other circuits in the BCII, such as the FU and MS-latch, may be turned off to save power.

The multimode routing method takes advantage of the FPGAs' reconfigurable feature. The memory configuration bits of an FPGA are also used to turn on/off a CML tree. In the new 4:1 multiplexer example of Fig. 1, the multiplexer's current tree control bit is an ORed function of the selection signals S1, S2, S3, and S4. If the MUX is not used, all selection bits are set to zero by memory bits. Then the CML tree will be turned off by its control bit.

Multimode routing circuits are implemented by CMOS. The circuit area and power consumption is much less than that of the active circuits of the BCII.

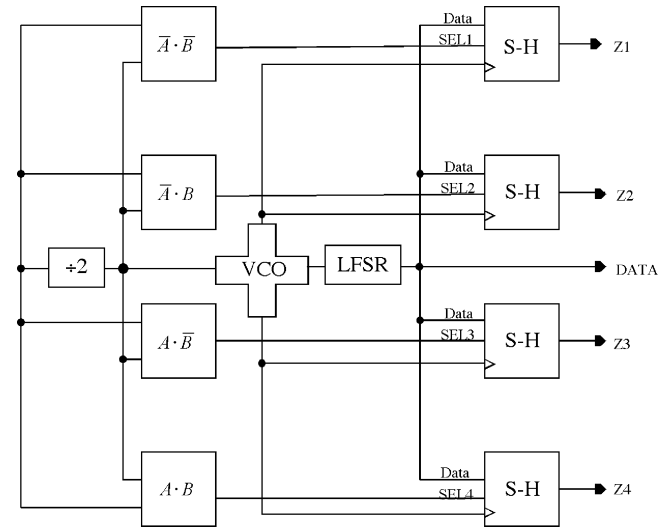

Fig. 4. 2×4 gate array–DEMUX chip schematic. The VCO generates the system clock. The 4-bit LFSR generates a pseudorandom bit pattern for testing purposes. The 2×4 gate array is configured to perform a DEMUX function. The left column of the gate array provides channel selection signals. The right column of the gate array captures data and provides data to the output pads.

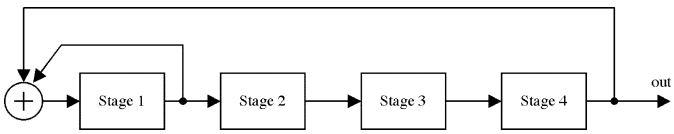

Fig. 5. 4-bit LFSR. Output of stage 1 and stage 4 are XORed as the input of stage one. The output from stage 4 is the LFSR output. The pseudorandom bit pattern is 15 bits wide: 000111101011001.

III. DEMUX IMPLEMENTED BY HIGH-SPEED FPGAS

Several chips have been fabricated to prove the combinational function performance and the power saving ideas [7], [8]. The last application that has been tested is a 12-Gb/s DEMUX implemented by the BCII structure in the IBM 7HP BiCMOS technology. The DEMUX, as shown in Fig. 4, contains a 2×4 FPGA gate array, a VCO, a 4-bit linear feedback shift register (LFSR), and input pads and output pads.

A. LFSR Design

An LFSR [9] is used to generate pseudorandom binary bits in this built-in self-test (BIST) design. State 0 (0000) is not permitted. Therefore, a maximum of 15 states can be obtained from this LFSR. The pseudorandom number comes from stage 4 as shown in Fig. 5. Each stage is a master-slave latch that shares the same system clock. To prevent all stages from being set to "0" at the time of power up, the output from stage 4 is inverted before it is fed back to stage 1.

B. Voltage Control Oscillator (VCO) Design

A VCO is used in this chip to provide the system clock for the LFSR and BCIIs. The VCO used here is a feed-forward interpolated VCO (FFI-VCO) [10], [11]. A block diagram of the VCO is shown in Fig. 6.

As shown in Fig. 6, each buffer stage has two inputs from the buffer preceding it and the buffer two stages preceding it. The buffer output is a mixture of both input signals. The VCO control signal controls the percentage of each input in the buffer output. For example, "B" has inputs from "A" and "D." "B" output has a certain percentage of the "A" and "D" signals. If each VCO buffer control heavily weights the outer "A" output, the VCO is a four-stage ring oscillator. If the VCO control favors the inner "D" input, the VCO behave as a two-stage ring oscillator. If the VCO input is somewhere in between, the VCO will output a signal frequency between those two extremes.

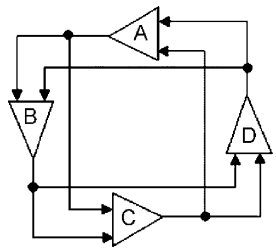

Fig. 6. Block diagram of an FFI-VCO. Each stage is a buffer with two inputs: forwarded and interpolated, i.e., buffer "B" depends on "A" and "D."

TABLE I
TRUTH TABLE OF THE 2:4 DECODER USED IN THE DEMUX TEST CHIP

A	B	SEL1	SEL2	SEL3	SEL4
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

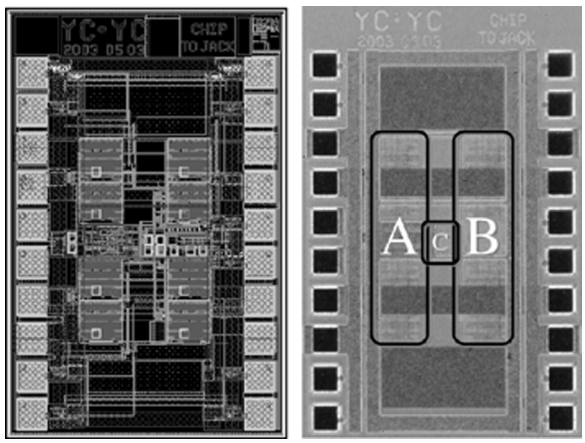

Fig. 7. Fabricated demultiplexer chip layout and photograph. Chip dimension is 1.09 mm × 1.68 mm. Area A is the 2-bit decoder. Area B is the four Select-Hold circuits. Area C is the VCO and LFSR.

C. FPGA Configuration

As shown in Fig. 4, the 2×4 gate array has been configured as a 1:4 DEMUX. The left column of the gate array is configured as a 2:4 decoder. This decoder is used to generate the selection signals. Table I shows the truth table.

Also, as shown in Table I, the frequency of signal "A" is half of the frequency of signal "B." Therefore, signal "A" is generated by a frequency divider from signal "B" in Fig. 8.

The right column of the 2×4 gate array is configured as four select-hold circuits. A DEMUX used in a receiver requires the holding feature to latch each channel's data until the next data-update cycle. The select-hold circuit is implemented by one BCII as shown in [8]. The MS latch is used in the select-hold circuit in order to hold the data. This configuration will prove the sequential function that has not been measured before. Four select-hold circuits can implement a 2:4 demultiplexer. The SEL signal comes from the outputs of the 2-bit counter. The LFSR and decoder share the same clock as with the MS latch. Each time, one SEL signal is asserted. The circuit updates its value one gate delay after the SEL is asserted. In the next clock cycle, the SEL is reset.

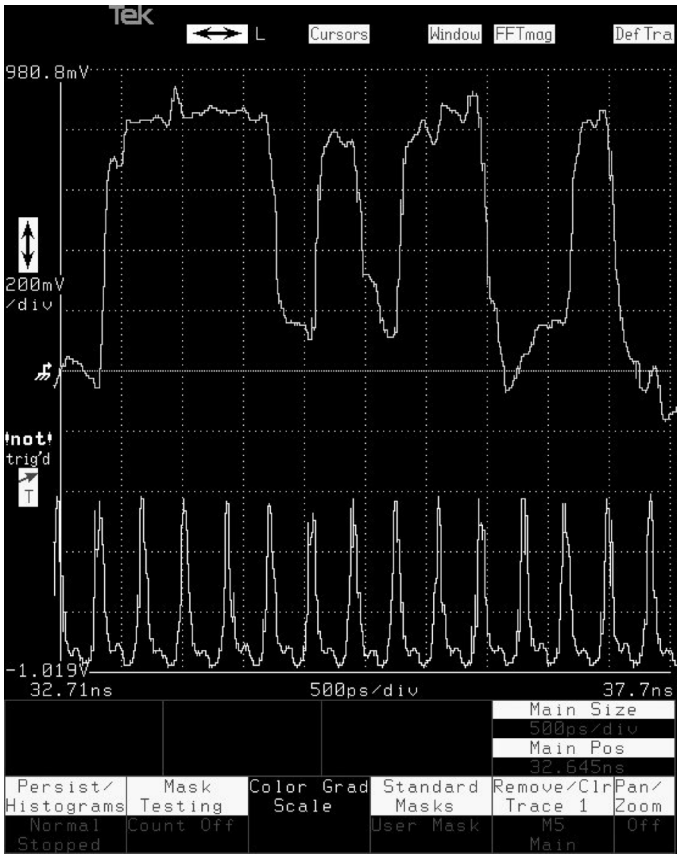

Fig. 8. Chip measurement of 11.6 Gb/s. Signal voltage swing is 900 mV. The signal is the channel Z1 data output (500 ps/div). The bit pattern shown in the figure is 011110101100100.

The circuit holds its value until the next time the SEL signal is asserted again.

D. Chip Simulation and Measurement

The chip was simulated at 27 °C. The center frequency of the VCO is 10 GHz. Because of the way the LFSR is designed, the corresponding LFSR generates a signal of 12 Gb/s. On each clock cycle, one of the SEL signals is enabled to turn on the Select-Hold circuit. Since the LFSR is synchronized with the VCO, data is synchronized with the SEL signals. Valid data is shown on the output side. The data from LFSR is also routed to an output pad so that the data can be compared with each channel's signal.

The fabricated chip is shown in Fig. 7. The chip area is $1.09 \times 1.68\ \text{mm}^2$. Twelve signal pads are used. Two VCO control signals are located on the left side of the chip. Four SEL signals are routed to the left side of the chip. Channel outputs, system clock, LFSR output, and clock trigger signals are routed to the right side of the chip.

The chip was measured at room temperature. Test power supply is 3.4 V. The current is 840 mA. Approximately 45% of the power is consumed by the input and output pads. Channel Z1 signal is shown in Fig. 8. The bit pattern read on the scope is "011110101100100," which is expected according to the LFSR simulation. The signal voltage swing is 900 mV. Channel A bit throughput is 2.9 Gb/s. Therefore, the DEMUX bit rate is 11.6 Gb/s.

In addition to the DEMUX configured in an FPGA in 7HP, faster applications can be implemented by the IBM 8HP SiGe BiCMOS FPGA. In the 210-GHz 8HP process, the simulated DEMUX has a data rate of 20 Gb/s. A 48×48 gate array in the IBM 8HP process has been submitted for fabrication. The onboard VCO is centered at 20 GHz. ADC/DAC circuits have also been added to the front and back end of the 20-GHz FPGA. More applications can be implemented in that high-speed FPGA, such as digital filters.

IV. Conclusion

This paper introduces circuits for a high-speed FPGA and an example application for sequential logic. These FPGA circuits have new features that have better performance, reduced power consumption, and increased routing capability. When fabricated by the IBM SiGe 7HP technology, the FPGA operates in the gigahertz range. One of the applications demonstrated here is a four-channel 12-Gb/s DEMUX. With the new IBM SiGe 8HP technology, circuit simulations operate in the 20 to 25 GHz range. More applications can be implemented using this faster high-speed SiGe kit.

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