

Wafer-Level In-Registry Microstamping

Albert Folch and Martin A. Schmidt

Abstract—Microstamping is an inexpensive technique that allows for micrometer-scale patterning of a rich variety of materials by a replication procedure based on an elastomeric stamp. We have investigated the scalability of microstamping for its use in the fabrication of microelectromechanical systems. Until now, the application of microstamping to multilayer processing at a wafer level has been impaired by the flexibility of the stamp. By mounting the stamp onto a rigid glass surface, we demonstrate the feasibility of in-registry multilayer microstamping at a 4-in wafer level. [287]

I. INTRODUCTION

THE IMPORTANCE of microelectromechanical systems (MEMS) for scientific and industrial applications is now widely recognized (for a review, see [1]). In our opinion, however, the MEMS research field is facing a crossroads. Presently, and generally speaking, MEMS researchers use microfabrication facilities that were built for the purpose of microelectronics processing. This imposes two major limitations. First, since the electronic properties of Si are very sensitive to dopant contamination, most materials (including most metals and their oxides, ceramics, and polymers, to name a few) are usually banned from clean-room laboratories. Second, in order to be compatible with photoresist spinning and exposure, substrates must be planar. This requirement constrains the design of three-dimensional structures and rules out surfaces with curvature, holes, and/or deep ($>15 \mu\text{m}$) trenches. Until now, MEMS researchers have circumvented these limitations with compromise and imagination, or by building dedicated facilities. But as the microelectronics industry pushes to increase wafer size (>8 in diameter) and resolution ($<0.3 \mu\text{m}$ linewidth), equipment and supplies are becoming increasingly expensive. However, small-area (≤ 4 in diameter) wafers and larger ($>1 \mu\text{m}$) linewidths are perfectly suited for most MEMS applications. Most importantly, MEMS are becoming research tools in areas such as physics, chemistry, or biomedicine, which cannot compromise on the materials used.

A family of patterning techniques recently developed by Whitesides *et al.* [2], [3], termed “microstamping,” allows for inexpensive micrometer-scale patterning of a rich variety of materials. With this technique, photolithography is needed only once to create a photoresist-patterned “master” wafer. A silicone-type mold replica is created by pouring a liquid prepolymer of polydimethylsiloxane (PDMS)¹ onto the master.

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¹The liquid is prepared by gently mixing two liquid components (Sylgard 184 kit, Dow Corning) in a 10:1 ratio by weight.

After thermal curing, the solidified PDMS replica or “stamp” is peeled away from the master. The stamp can be used in a variety of ways to replicate its features by contact-transfer of certain materials from the stamp onto a surface (which need not be planar [4], [5]) only on the areas contacted by the stamp. Alternatively, a precursor fluid can be “micromolded” into the stamp channels and cured or dried onto a substrate on the areas that do *not* contact the stamp [6], [7]. The concept is particularly versatile because, due to the stamp’s inert and elastomeric nature, it easily releases the material to be transferred and it is not damaged by the stamping procedure [3].

It is well proven that microstamping is capable of submicrometer resolution [3]. The motivation for the present work was to investigate its capabilities for MEMS fabrication, i.e., for patterning *large* (5–5000 μm) features over wafer-wide areas and for multilayer patterning over surfaces containing deep features such as those frequently present in MEMS devices. In practice, the problems that one encounters are that a) the flexibility of the stamp causes feature distortions and severely impairs registry (i.e., preservation of periodicity) during alignment (i.e., adjustment of the orientation of one wafer with respect to the other); b) noncontact areas of fractions of 1 mm^2 and greater are prone to collapse during separation from the sample as curvature is induced on the stamp; and c) in general, microstamping over areas larger than several cm^2 is affected by bubble trapping during the contact-transfer procedure². We emphasize that solving these issues is a prerequisite for the application of microstamping techniques to multilayer patterning of planar surfaces.

II. EXPERIMENTAL METHODS

Our stamps consist of a thin ($\sim 500 \mu\text{m}$) layer of PDMS cured between a 4-in-diameter photoresist-patterned Si master and a rigid glass piece, as depicted in Fig. 1. The thickness of the PDMS layer is determined by a set of spacers between the glass piece and the master wafer. The master is separated from the PDMS/glass by levering with a sharp wedge inserted (~ 3 –5 mm) between them. The thin layer of PDMS remains adhered to the glass piece. We observed that the separation force is mask dependent and is greatly reduced when the master is prepared from inert substrates such as Si_3N_4 - or Au-coated Si wafers. The photoresist profile and total wall area are probably responsible for the dependence of separation force on specific mask design. The improved rigidity of our stamps prevents large noncontact areas from collapsing and

²An original solution to the problem of bubble formation consists in mounting the stamp in a roller, but the alignment problem persists; for details, see [8].

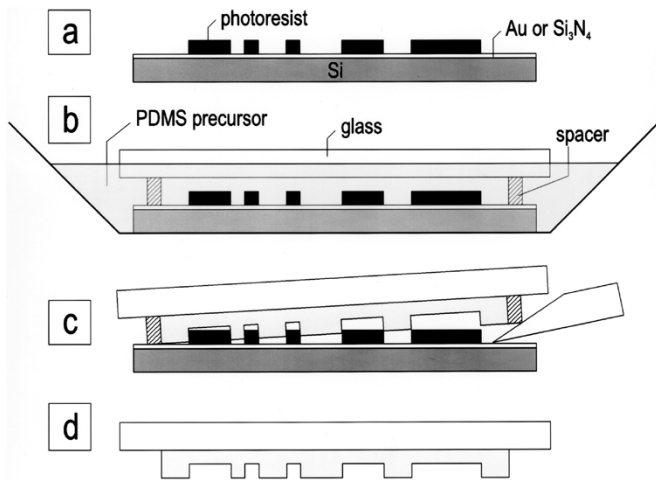


Fig. 1. Cross section schematics of stamp fabrication. (a) A “master” wafer is prepared by photolithographic patterning of photoresist (1–6 mm thick) on a Au- or Si_3N_4 -coated Si wafer; a glass piece with a set of spacers ($\sim 750 \mu\text{m}$ thick) is pressed against the master until the spacers come into contact with the master; PDMS is allowed to cure at 60°C for 4 h; (c) the PDMS/glass is separated from the master by levering with an inserted wedge; and (d) the spacers are removed.

allows: 1) application of moderate pressures for displacing air bubbles trapped during the contact procedure and 2) in-registry patterning by minimizing lateral distortions of the features, as shown below.

In the original work by Kumar *et al.* [2], the stamp was used to “print” hexadecanethiol molecules ($\text{CH}_3-(\text{CH}_2)_{n-1}-\text{SH}$, $n = 16$) onto a gold-coated surface only on the areas that contact the stamp. It is now well established that, via bonding of the sulfur end to the metal surface, long-chain alkanethiols ($n > 9$) spontaneously form close-packed “self-assembled” monolayers (SAM’s) on clean Au, Ag, or Cu [9], [10]. Interestingly, patterned SAM’s can be used as a submicrometer-resolution mask for a cyanide-based selective Au, Ag, or Cu etch [3], [11] or as a template of differential wettability or catalytic activity for the subsequent formation of patterns of metals [3], [4], liquids [12], [13], crystals [3], polymers [3], [14], or proteins [15]. Obviously, thiol microstamping is limited to Cu-, Ag-, or Au-coated substrates; on the other hand, due to its inertness, Au is suitable for masking most chemical etches. In all the experiments presented here, the stamp was inked with a ~ 1 mM solution of hexadecanethiol in ethanol using a cotton tip, dried in air, brought into contact with a Au- or Ag-coated 4-in-diameter wafer for a few seconds, and carefully pulled apart from the substrate [3]. The exact molarity of the solution is not important, since the ethanol evaporates and only a small fraction of molecules effectively contribute to the completion of the SAM. The stamped substrate was thoroughly rinsed with ethanol and blow-dried prior to further processing. All experiments were performed outside of the clean room in a conventional fume hood.³

We used the aqueous ferro/ferricyanide etch of Au and Ag

developed by Xia *et al.* [11].⁴ In the case of the Ag etch, which is about ten times faster than that of Au, timing of the etch is critical. Alkanethiol SAM’s, whether due to the underlying polycrystalline Au/Ag topography, to impurities adsorbed before formation of the SAM, or to incomplete self-assembly, present nanometric defects or “holes” [16], [17]. During a SAM-masked etch, the etching solution penetrates the holes and transfers them onto the metal layer. In practice, since the etch produces amplification of the holes, the etch selectivity is determined by the hole density and is not improved by using thinner metal films. For our large-area SAM/Au or SAM/Ag substrates, the selectivity is further reduced due to a significant distribution of etch rates across the 4-in wafer (20–30 $\text{\AA}/\text{s}$ for Ag), likely due to diffusion limitations in our ~ 1 L containers and manual stirring conditions. This effectively increases the time needed to complete the etch over the whole wafer. We found that 15 s of Ag etch under agitation for a 500 \AA -thick Ag film results in acceptable yields, as shown below.

We were able to superimpose the stamp pattern, which we name *B*, in registry with an underlying pattern, *A*. Both patterns feature the same nominal periodicities (3500 μm in the *x* direction and 3600 μm in the *y* direction). We refer to each 3500 $\mu\text{m} \times 3600 \mu\text{m}$ repetitive unit area as a “chip.” A portion of each pattern is shown schematically in Fig. 2(a) to depict the superimposition procedure. To avoid cancellation of systematic errors, pattern *A* was created by conventional photolithography on an Si_3N_4 -coated (1500 \AA) Si(100) wafer; thus, for our purpose, it has perfect periodicity. Each *A* chip contains, among other features, a 975 $\mu\text{m} \times 2600 \mu\text{m}$ opening in the Si_3N_4 layer which was used to mask a through-wafer KOH etch, resulting in a cavity with (111)-oriented sidewalls. Note the $\sim 8 \mu\text{m}$ undercut in the Si_3N_4 layer at the edges of the cavity as a result of lateral etch. The etched wafer was then coated with $\sim 500 \text{\AA}$ of Ag and pattern *A* was defined on the Ag layer by alkanethiol microstamping and ferro/ferricyanide selective etching of Ag (~ 15 s) on the nonstamped areas. A portion of the resulting bilayer pattern is shown in Fig. 2(b). The relevant features in pattern *B* are a set of squares in decreasing sizes ranging from 20 μm - to 9 μm -side. Notice the slight rounding of all (concave as well as convex) corners, possibly caused by reactive spreading of alkanethiols [18]. It should also be observed that the Ag pattern reaches the edge of the 1500 \AA -thick Si_3N_4 undercut and that, probably due to bending of the unsupported Si_3N_4 , the squares are slightly deformed. Furthermore, we highlight that Fig. 2 exemplifies a solution to an acute problem in MEMS fabrication, i.e., electrode patterning over deep nonplanar structures. Although microstamp separation from the sample requires applied force that could potentially result in wafer cracking, our wafers containing numerous through-wafer cavities did not pose any problems.

III. REGISTRY MEASUREMENTS

For simplicity, the stamp is positioned by hand. Therefore, the two patterns are slightly misaligned. Note that two patterns

³ Handling of the wafers outside of the clean room may result in occasional scratches [see Fig 3(a)] due to particles.

⁴ We add 19 g of $\text{K}_2\text{S}_2\text{O}_8$, 3.3 g of $\text{K}_3\text{Fe}(\text{CN})_6$ and 0.4 g of $\text{K}_4\text{Fe}(\text{CN})_6$ to 1 liter of KOH 1 M. All chemicals were obtained from Aldrich.

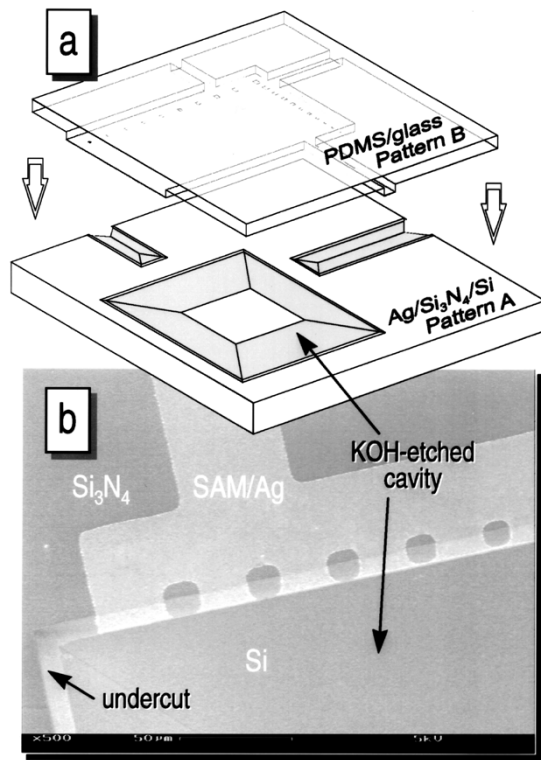


Fig. 2. (a) The PDMS stamp (top) is used to microstamp a pattern B of hexadecanethiol SAM onto an Ag-coated (~ 500 Å) substrate (bottom) containing a pattern A previously defined by photolithography and Si_3N_4 -masked KOH etch and (b) SEM image of the substrate after microstamping and selective etching of Ag on the nonstamped areas. Note that the Ag layer is patterned to the very edge of the Si cavity, where the Si_3N_4 layer is undercut by ~ 8 μm .

do not need to be aligned in order to demonstrate registry: it is sufficient to prove that they *would* be in registry if they were aligned. All distances were measured digitally from SEM images and registry verified by simple vector algebra, as follows. In the examples shown in Fig. 3, the resolution was 0.9 $\mu\text{m}/\text{pixel}$. Since both patterns have the same periodicity, pairs of equivalent points A_i and B_i , belonging to layers A and B , respectively, may be identified on each chip i with different relative positions \vec{R}_i

$$\vec{R}_i = (B_{ix} - A_{ix}, B_{iy} - A_{iy})$$

as depicted in Fig. 3. The x and y axes are defined parallel to the axis of symmetry of the chip and their orientation determined independently from each SEM image. First, we measure \vec{R}_1 in an arbitrarily chosen chip 1 [Fig. 3(a)]. Point A_1 is defined as the origin, i.e., $A_1 = (0, 0)$. Equivalent points A_2 and B_2 defining \vec{R}_2 can be found in a distant chip 2 [Fig. 3(b)]. Assuming that the photolithographically defined pattern A has perfect registry, the absolute position (in micrometers) of A_2 can be expressed as $(m \times 3500, n \times 3600)$, where m and n are the integer number of units that separate chip 1 from chip 2 in the x and y direction, respectively. Then $B_2 = A_2 + \vec{R}_2$. In the event of perfect registry, the distance D_B between B_1 and B_2

$$D_B = \sqrt{(B_{2x} - B_{1x})^2 + (B_{2y} - B_{1y})^2}$$

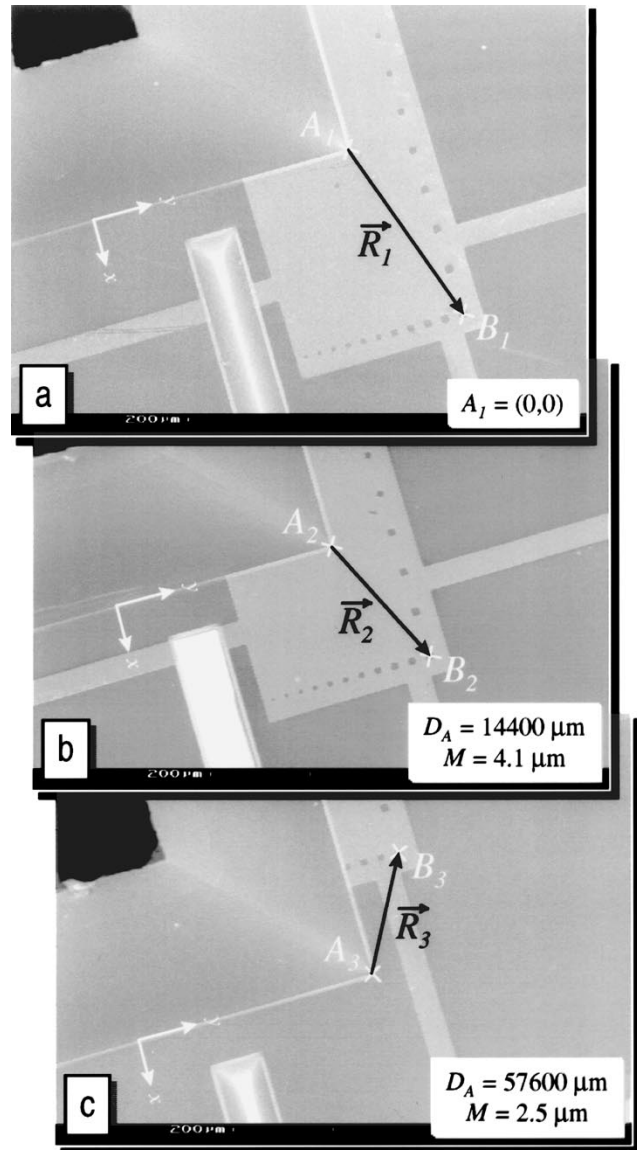


Fig. 3. SEM micrographs showing our method of measurement of misregistry M between pattern A and B . (a) The relative position \vec{R}_1 of two points A_1 and B_1 belonging to patterns A and B , respectively, is measured in an arbitrarily chosen reference chip and compared with the relative positions \vec{R}_i of equivalent points A_i and B_i in other chips [such as shown in (b) and (c)] at a distance D_A from the reference chip to compute a misregistry value M (see text for details).

should be the same as the distance D_A between A_1 and A_2

$$D_A = \sqrt{(m \times 3500)^2 + (n \times 3600)^2}.$$

Therefore, the quantity $M = |D_B - D_A|$ is a good scalar measure of misregistry between chips 1 and 2. This same analysis is repeated for many other chips. Over the longest chip column, with 19 chips and a length of around 7 cm (as we are limited by the SEM stage travel), for the wafer in Fig. 3 the average and maximum M were 1.46 and 4.08 μm , respectively. Similar values were obtained for other wafers. Our largest source of error is pixelation. Given our resolution of 0.9 $\mu\text{m}/\text{pixel}$ and taking error propagation into account, these deviation values are surprisingly low. An error of ± 1 pixel in the measurement of B_{1y} , for example, yields an

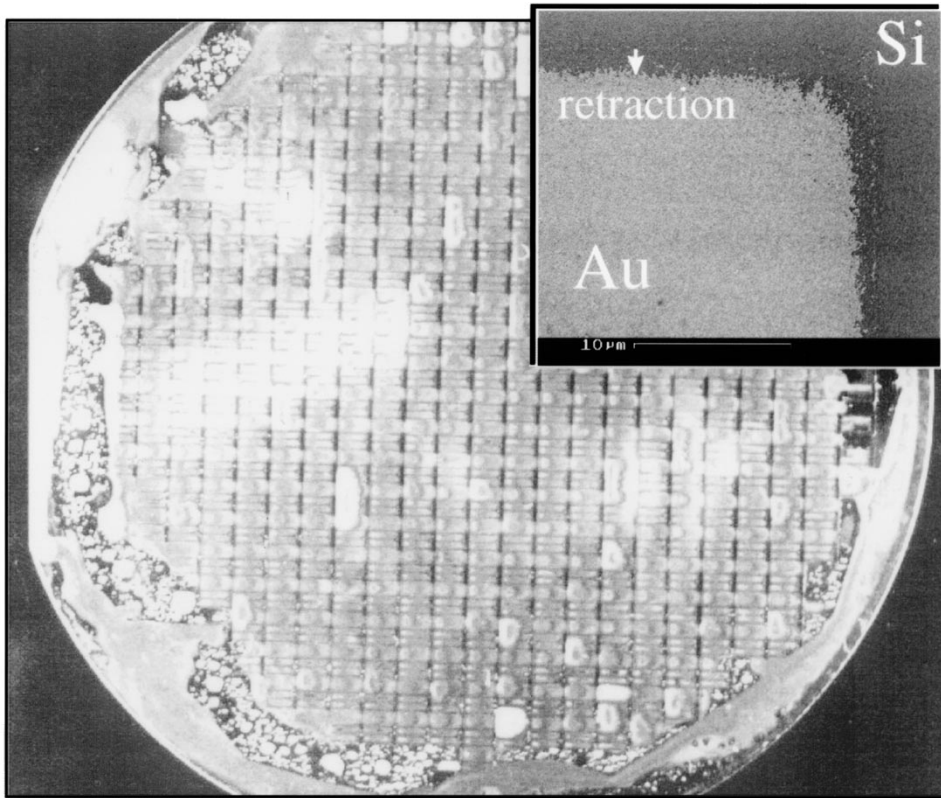


Fig. 4. Optical picture showing a pattern of sprayed water-based polyurethane which dewetted 95% of a 4-in-diameter Au-coated Si wafer microstamped with hexadecanethiol. The exposed Au areas were etched with a 10:8:1 $\text{H}_2\text{O}:\text{HCl}:\text{HNO}_3$ solution, which did not attack the PU mask. Typical line and corner definition after the Au etch are shown in the inset SEM picture. The PU edge retracted by $\sim 1 \mu\text{m}$ during drying.

error in D_B of $\pm 0.5 \mu\text{m}$. Since each M value involves the determination of the x and y position of eight points in two SEM images (A_1, A_2, B_1, B_2 , and two points on each image to find the orientation of the y or x axis), one would expect deviation values on the order of $\pm 8 \mu\text{m}$ even in the event of perfect registry. We can only conjecture that, in practice, since we always aim for equivalent points in the same pattern, we consistently pick the same pixel relative to that pattern, which effectively lowers the pixelation error. In any case, our results demonstrate that our rigid-plate-mounted stamps are suitable for alignment in registry with an upper limit for the misregistry values of $\sim 60 \text{ nm per mm}$, that is, with an accuracy better than $5 \mu\text{m}$ over the whole area of a 4-in wafer. This value is satisfactory for most MEMS applications.

IV. POLYURETHANE PATTERNING

Gold films are not ideal for masking isotropic deep Si etches because residual stress causes them to peel off at the overhanging edges. Certain polymer masks may be used instead. Similarly to Kumar *et al.* [3], we used the wetting properties of microstamped SAM's to make polymer patterns on Au-coated Si. After microstamping an alkanethiol pattern, the wafer is exposed to a liquid precursor of the polymer which dewets only the microstamped areas. The pattern solidifies upon UV or thermal curing or drying. However, we found that for our large wafers, the polymers used in [3] dewet as little as 40–60% of the stamped area, depending on the pattern design and orientation. Since dewetting is assisted by gravity,

the areas which fail to dewet are concentrated at the bottom half of the wafer. Instead, we used water-based polyurethane (PU)⁵ and sprayed it for $\sim 0.5 \text{ s}$ onto a horizontally oriented wafer with a paint gun to obtain uniform coverage. The wafer dewetted successfully on $\sim 95\%$ of its stamped areas, as shown in Fig. 4. We hypothesize that, due to nonspecific adsorption of impurities or the PU precursor itself on the wafer surface, the wettability differential between thiol-covered and exposed Au areas decreases, in a time scale of a few seconds, as the time of exposure to the PU solution increases. With our spraying procedure, a microdroplet falling on a hydrophobic region is immediately repelled to a nearby hydrophilic region without having to flow over the whole wafer. This hypothesis is consistent with the observation that gravity-assisted dewetting fails mostly at the wafer bottom.

V. CONCLUSION

In conclusion, we demonstrated an improvement of the lateral rigidity of the stamps which allowed us to perform in-registry microstamping, with misregistry values on the order of 60 nm per mm or better. We also implemented solutions for yield enhancement in alkanethiol-masked PU dewetting over a 4-in wafer. We believe that simple strategies for making masks, such as the incorporation of lines to assist in dewetting or in displacing trapped bubbles, would further maximize the yield. We conclude that microstamping is a viable technique for wafer-level multilayer patterning in MEMS, especially

⁵SCL Co, Malden, MA. We diluted it 3:1 in deionized water.

attractive for inexpensive prototype development in university laboratories.

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